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PLATED WIRE RANDOM ACCESS MEMORIES

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June 1975 FINAL REPORT FOR PERIOD June 1974 - June 1975

Prepared for GODDARD SPACE FLIGHT CENTER Greenbelt, Maryland 20771

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FINAL REPORT

PLATED WIRE RANDOM ACCESS MEMORIES

June 1975 for period June 1974 - June 1975

Contract No. NAS 5-20576
for
GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland 20771

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ATTACHMENTS: PREFACE: Prior to Table of Contents

ATTACHMENT I: ACCEPTANCE TEST PROCEDURE (35 Pages)

ATTACHMENT II: ACCEPTANCE TEST DATA SHEETS S/N 103 (35 Pages) ATTACHMENT III: ACCEPTANCE TEST DATA SHEETS S/N 104 (35 Pages) ATTACHMENT IV: ACCEPTANCE TEST DATA SHEETS S/N 105 (35 Pages)

ATTACHMENT V: ACCEPTANCE TEST DATA SHEETS S/N 106 (35 Pages)

REV.	ву	APPROVED	DATE	DESCRIPTION
	SLT	See Title Page	6/25/75	Initial Issue

PREFACE

This Final Report documents the work done under NASA Contract NAS-5-20576 by Motorola, Inc., Government Electronics Division for the Goddard Space Flight Center, Greenbelt, Maryland. The work performed under the subject contract entailed the construction and testing of a 4096-words by 18-bits Random Access, NDRO-Plated Wire Memory. Four memory units were delivered to Goddard. This report gives the performance requirements, construction, and test history of the units along with a complete technical and functional description. The report covers the period from June 1974 through June 1975.

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SECTION 1

INTRODUCTION AND OVERALL PROGRAM SUMMARY

1. INTRODUCTION

This Final Engineering Report documents the overall activity and history of the work performed by Motorola Inc., Government Electronics Division, Scottsdale, Arizona for the Goddard Space Flight Center, Greenbelt, Maryland, under NASA Contract No. NAS 5-20576. The report is submitted in accordance with the requirements of Specifications 73-15079 modified June 1974 and the addendum dated May 1974, and covers the period from June 1974 through June 1975.

1.1 PROGRAM SUMMARY

The work performed under the subject contract entailed the construction and testing of a 4096-word by 18-bit Random Access, NDRO-Plated Wire Memory.

The primary design parameters, in order of importance, were:

- High reliability
- Low power
- Volume
- Weight

Four memory units, serial no. 103, 104, 105, and 106 were delivered.

1.2 RESULTS ATTAINED

The memory units were subjected to comprehensive functional and environmental testing at the end-item level to verify comformance with the specified requirements.

A comparison of the memory unit's most significant physical and performance characteristics versus the specified requirements is shown in Table 1.

Table 1. Memory Performance Versus Specified Requirements

Characteristic	Contract Reference	Specified	Measured
Volume	73-15079	160 in ³	158, 5 in ³
Weight	73-15079 Mod 6/20/74	5.8 Pounds	5. 640 pounds (SN103) 5. 562 pounds (SN104) 5. 594 pounds (SN105) 5. 580 pounds (SN106)
F=@er Operate	73-15079 Mod 6/20/74	7 watts	5. 963 watts max (SN103) 5. 914 watts max (SN104) 5. 324 watts max (SN105) 5. 687 watts max (SN106)
Power Standby	73-15079	170 milliwatts	149 milliwatts max (SN103) 147-milliwatts max (SN104) 139 milliwatts max (SN105) 147 milliwatts max (SN106)
Voltage Tolerance	73-15079	±5% on all	±5% on all
Operating Rate	73-15079	500 kHz	600 kHz
Access Time	73-15079	500 nanoseconds	<500 nanoseconds
Operating Temp.	. 73-15079	-40°C to +85°C	Tested from -40°C to +85°C
Operating Vacuum	73-15079 Mod 6/20/74	One atm. to 10 ⁻⁵ mm Hg modified for test purposes.	Tested from one atm. to 10^{-5} mm Hg.

Table 1. Memory Performance Versus Specified Requirements (Contd)

Characteristic	Contract Reference	Specified	Measured
Operating Vibration	73-15079	Sinusoidal	Tested at specified levels
	Mod 6/20/74	5.25 Hz33 in da	
		25-110 Hz-10g Peak	
		110-2000 Hz-5g	
		Peak Two octaves/	
		minute	
		Random	
		15 Hz,.0004 g ² /Hz	
		15-70 Hz,	
		Linear Increase	
		70-100 Hz,	
		$0.138 \text{ g}^2/\text{Hz}$	
		100-400 Hz	
		Linear Decrease	
		400-2000 Hz,	
		$0.0089 \text{ g}^2/\text{Hz}$	
		Two min/axis	
Operating Shock	73-15079	Two shock pulses	Tested at specified levels
		of 30g for 6 and	
		12 milliseconds	
		in three axis	

SECTION 2

HISTORICAL PROGRAM SUMMARY

2. PROGRAM HISTORY

The design modification, construction, and test history, as related to the hardware requirements of this contract, is summarized in this section.

Four low-power random access spacecraft memories were constructed, tested, and delivered under this contract. The memories were constructed using the same basic design as units SN101 and SN102, previously delivered under contract no. NAS5-23163, with slight modifications. The word current generator was changed from a hybrid circuit to a discrete circuit which required a new layout of the timing and control board. The housing material was changed from aluminum to magnesium and the mu-metal magnetic shielding was removed to reduce the overall weight of each unit.

The initial contract was for three memory units with an option for two follow-on units. On 9/23/74 the contract was modified to exercise the option on the fourth memory unit and revise delivery schedule due to repair of a memory unit previously delivered under contract no. NAS 5-23163 which had been subjected to over temperature at GSFC.

The summarization is in chronological order from date of contract award to date of final delivery of the memory units.

2.1 SERIAL NUMBER 103

Assembly was completed and system testing began in January 1975. On 2/6/75 GSFC reported they had found a wire bond problem while performing construction analysis on the single digit driver hybrid circuits. Construction analysis at Motorola confirmed the problem and traced the cause to contamination of the gold plating on the single digit driver package. New packages were procured, tested for gold purity, and new single digit driver hybrids were constructed. The new single digit driver hybrids were installed in March 1975 and system test resumed.

Several minor destan modifications were recommended to GSFC in April 1975 to improve waveform timing tolerances due to capacitance differences with the new Timing and Control board layout and to reduce power consumption. These modifications were approved by GSFC and incorporated in all units.

The unit was acceptance tested and shipped to GSFC on May 13, 1975.

2.2 SERIAL NUMBER 104

Assembly was completed and system testing began in April 1975. Due to bit errors during stack test and system test Serial Number 105 advanced ahead of SN104. Acceptance testing was completed on June 9, 1975 and shipped to GSFC.

2.3 SERIAL NUMBER 105

Assembly was completed and system testing began in May 1975. During acceptance test three failures occurred. GSFC Malfunction Reports were written and submitted to GSFC.

The first failure was a marginal level bit error which occurred during worst case pattern testing at -40° C and was corrected by replacing a wire pair. Reference GSFC MRF No. D07898.

The second failure was again a marginal level bit error which occurred during worst case pattern testing. This error occurred during the intermediate temperature test after the -40° C testing had been completed. The error was corrected by replacing a wire pair. Reference GSFC MRF No. D07899.

The third failure also occurred at cold temperature. This time a complete digit pair was bad due to a film of flux on one of the connector pins. Reference GSFC MRF No. D078900. The connector pins were cleaned and the unit confidence tested at cold temperature. Temperature testing per the acceptance test procedure was repeated and the unit shipped to GSFC on May 30, 1975.

2.4 SERIAL NUMBER 106

Assembly was completed and system testing began in May 1975. The unit failed cold temperature test due to an unsoldered pin on I/C U5 on the Timing and Control Board. GSFC Malfunction Report No. D09085 was written and submitted to GSFC. Acceptance testing was completed and the unit was shipped to GSFC on June 26, 1975.

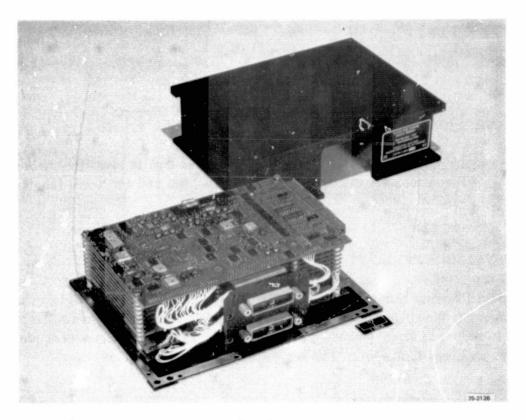


Figure 1. 4K x 18 Bit Plated Wire Memory System

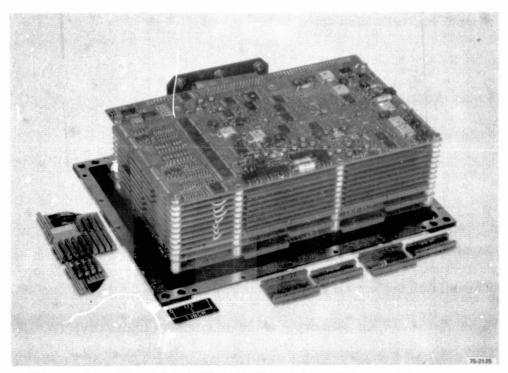


Figure 2. $4K \times 18$ Bit Plated Wire Integral Assembly

SECTION 3

TECHNICAL DESCRIPTION

3. DESCRIPTION

The memory unit is shown in Figures 1 and 2. The unit is identified as Motorola Part Number 01-P13701D002. Serial Numbers 103, 104, 105 and 106 were fabricated, tested & delivered.

3.1 SYSTEM CONFIGURATION

Motorola Drawing Numbers 01-P13701D, 15-P13745D, and 15-13746D (included in the engineering drawing package submitted to GSFC) completely define the end-item package in terms of size, mounting pattern, etc. The external connector pin assignments are as given in Table 2. The weight of each delivered unit was <5.8 pounds.

3.2 ELECTRICAL INTERFACE

Connectors J1 and J2 are Deutsch, Type 75020-442P, as modified and supplied by GSFC. The total memory interface is comprised of the following (Refer to Figure 3 Memory System Electrical Interface):

- 18 Input Data Lines (to memory)
- 16 Input Address Lines (to memory)
- 18 Output Data Lines (from memory)
- 1 Initiate Line (to memory)
- 1 Read/Write Select Line (to memory)
- 1 Read Complete Line (from memory)
- 2 Thermistor Sensor Lines (from memory)
- 7 Lines for -6.1V (to memory all lines common internally)
- 5 Lines for +5.0V (to memory all lines common internally)
- 12 Lines for Power and Signal Return (all lines common internally)

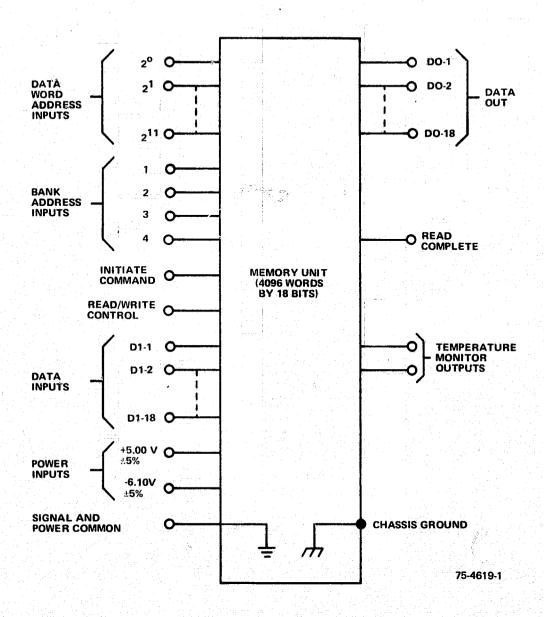


Figure 3. Memory System Electrical Interface

All signal inputs and outputs are to, or from, TTL Series 54 Standard logic devices. All inputs present one unit load. There is no internal loading on any of the output signal lines. The 18 data output lines and the read complete line are driven from open collector logic elements whose output transistor is normally in the OFF state.

The electrical interface characteristics of the delivered unit are as follows. On all signal inputs, a logic ONE is defined as the most positive voltage level, with respect to the return. On all signal outputs, a logic ONE is defined as the high impedance state. All time relationships are defined from the 50 percent points of the respective signals. Transition times (where applicable) are as specified for TTL Series 54 Standard logic with loading as applied. Stability is defined as being above the minimum logic ONE level or below the maximum logic ZERO level.

Memory Capacity: 4096 words of 18 bits each (73,728 bits total).

Access: Random by word via 12-bit input address. Also provides for addressing by memory unit via four-bit bank address. All bank address bits must be at a logic ONE for access.

Access Time: 500 nanoseconds, maximum, from leading edge of Initiate signal.

Read Cycle Time: 1.20 microseconds, maximum, from leading edge of Initiate signal.

Write Cycle Time: 1.00 microseconds, maximum, from leading edge of Initiate signal.

Operate Rate: 0 to 600k operations per second, minimum, with any read/write ratio.

Initiate Signal: Active level = logic ONE. Minimum pulse width = 50 nanoseconds.

Maximum pulse width = 450 nanoseconds.

Read/Write Select: Read = logic ONE. Write = logic ZERO. Must be stable from leading edge of Initiate signal to end of read or write cycle.

()

Bank Address Lines: Must be stable from leading edge of Initiate pulse to end of Read or Write cycle.

Word Address Lines: Must be stable from leading edge of Initiate to end of cycle time.

Table 2. External Connector Pin Assignments

Pin No.	Function	Pin No.	Function
J1-1A	Address Bit 2	J2-1A	Data Input Bit 2 ⁰
-1B	Address Bit 21	-1B	Data Input Bit 2 ¹
-1C	Address Bit 2 ²	-1C	Data Input Bit 2 ²
-1D	Address Bit 2 ³	-1D	Data Input Bit 2 ³
-1E	Address Bit 24	-1E	Data Input Bit 2 ⁴
-1F	Address Bit 2 ⁵	-1F	Data Input Bit 2 ⁵
-1G	Address Bit 2 ⁶	-1G	Data Input Bit 2 ⁶
-1H	Return	-1H	Data Input Bit 2 ⁷
-1J	Read/Write Control	-1J	Data Input Bit 2 ⁸
-1K	Return	-1K	Data Input Bit 2 ⁹
-1L	Return	-1L	Data Input Bit 2 ¹⁰
-1M	Return	-1 M	Data Input Bit 2 ¹¹
-1N	Initiate Command	-1N	Data Input Bit 2 ¹²
-1P	Not Assigned	-1P	Data Input Bit 2 ¹³
-2A	Address Bit 2 ⁷	-2A	Data Input Bit 2 ¹⁴
-2B	Address Bit 2 ⁸	-2B	Data Input Bit 2 ¹⁵
-2C	Address Bit 2 ⁹	-2C	Data Input Bit 2 ¹⁶
-2D	Address Bit 2 ¹⁰	-2D	Data Input Bit 2 ¹⁷
-2E	Address Bit 2 ¹¹	-2E	Data Output Bit 2 ⁰
-2F	Bank Address Bit 0	-2F	Data Output Bit 2 ¹
-2G	Bank Address Bit 1	-2G	Data Output Bit 2 ²
-2H	-6.1V	-2H	Data Output Bit 2 ³
-2 J	-6.1V	-2J	Data Output Bit 2 ⁴
-2K	-6. 1V	-2K	Data Output Bit 2 ⁵
-2L	-6.1V	-2L	Data Output Bit 2 ⁶
-2M	-6.1V	-2M	Data Output Bit 2 ⁷
-2N	-6.1V	-2N	Data Output Bit 2 ⁸

Table 2 External Connector Pin Assignments (Contd)

			
Pin No.	Function	Pin No.	Function
J1-2P	-6.1V	J2-2P	Data Output Bit 2 ⁹
-3A	Bank Address Bit 2	-3A	Data Output Bit 2 ¹⁰
-3B	Bank Address Bit 3	-3B	Data Output Bit 2 ¹¹
-3C	+5.0V	-3 C	Data Output Bit 2 ¹²
-3D	+5,0V	-3D	Data Output Bit 2 ¹³
-3E	+5.0V	-3E	Data Output Bit 2 ¹⁴
-3F	+5.0V	-3F	Data Output Bit 2 ¹⁵
-3G	+5.0V	-3 G	Data Output Bit 2 ¹⁶
-3H	Thermistor	-3H	Data Output Bit 2 ¹⁷
-3J	Thermistor	-3J	Return
-3K	Read Complete	-3K	Return
-3L	Return	-3L	Return
-3M	Return	-3 M	Return
-3N	Not Assigned	-3N	Return
-3P	Not Assigned	-3P	Return

Input Date Lines: For write operations, must be stable from leading edge of Initiate to end of cycle time. For read operations, may be any level within TTL logic limits.

Read Complete Line: Presents high impedance (20k minimum) in quiescent state. Goes active (i.e. low impedance) at end of access time (maximum of 500 nanoseconds following leading edge of Initiate signal). Remains at active level for minimum of 250 nanoseconds and maximum of 450 nanoseconds. Will sink minimum of 10 mA at 0.3V in active state.

Data Output Lines: Presents high impedance state (20k minimum) in quiescent state.

Goes active (i.e. low impedance) prior to or in coincidence with the leading edge of Read Complete signal and remains active for minimum of 150 nanoseconds following trailing edge of Read Complete signal and maximum of 750 nanoseconds. Will sink minimum of 10 mA at 0.3 V in active state.

3.2.1 Power Source Requirements

The memory unit operates from power sources of +5.0V and -6.1V. Requirements imposed on these power sources by the memory are as follow (all measurements made at connector terminals):

+5/0V:

Regulation: ±5%

Average Standby Current: 12.2 mA, worst-case.

Average Operate Current: 795 mA, worst-case at operate rate of 500k operations per second and read/write ratio of one.

Standby Power: 64.1 milliwatts maximum at +5.25V.

Operate Power: 4.171 watts, maximum, at +5.25V and at operate rate of 500 kHz with a read/write ratio of one.

-6.1V:

Regulation: ±5%

Average Standby Current: 14.5 mA, worst-case.

Average Operate Current: 280 mA, worst-case at operate rate of 500k operations per second and read/write ratio of one.

Standby Power: 92.8 milliwatts, maximum, at -6.40 volts.

Operate Power: 1.792 watts, maximum, at -6.40 volts and at operate rate of 500 kHz with read/write ratio of one.

3.2.2 Thermistor Characteristics

The thermistor is mounted at the approximate center of the unit. It is a YSI Type 44006 precision element with a nominal impedance of 10k ohms at +25°C. The resistance versus temperature characteristic is given in Table 3.

TEMPERA 80°C to +150°C TEMPOC RES TEMPOC RES TEMPOC RES TEMPCC RES TEMPOC RES TEMPOC RES TEMPOC RES TEMPOC RES --50 49 --20 19 18 17 3558K 3296K +10 11 18 79 K 17.98 K 441,3K 78.91 K -80+40 5592 十70 71 1990 1928 816.8 +130 131 +100 376,4 79 414.5K 74.91K 5389 101 794 6 367.4 78 3055K 18 389.4K 71.13K 12 13 17.22K 42 5193 72 1868 773.1 132 358.7 77 2833 K 47 366.0K 67.57K 16.49K 43 44 5006 73 1810 103 752.3 133 350.3 76 45 45 44 16 15 2629 K 344.1K 64.20K 14 15,79 K 4827 1754 704 732.1 134 342.0 75 61.02K 58.01K 75 76 77 78 2440K 323.7 K 15 16 15.13K 45 4655 1700 135 136 105 712.6 334.0 14 74 2265 K 304.6K 14 50K 13,90K 46 47 4489 1648 106 693.6 326.3 43 42 41 73 72 2106K 13 55.17K 17 286.7 K 4331 1598 107 675.3 137 318.7 12 1957K 270,0K 52 48 K 13.33K 48 4179 18 1549 108 657.5 640.3 138 311.3 71 1821K 254.4K 49,94K 19 12.79K 49 79 4033 1503 139 304.2 -40 --70 1694K 239.8K -1047.54K 12.26 K 11.77 K 3893 3758 +20 21 22 23 24 25 26 27 28 29 +50 51 52 53 54 55 56 57 58 59 +80 1458 +110 623.5 +140 297.2 39 38 37 36 69 1577K 226.0K 9 45.27K 81 82 83 1414 111 607 3 141 290.4 68 1469K 213.2K 8 43.11K 11.29K 3629 1372 112 591.6 142 283.8 67 1369 K 201.1K 41.07K 10.84K 3504 1332 113 576.4 143 277.4 66 1276K 189.8K 39,14K 84 85 86 10.41K 3385 1293 561 6 144 114 271.2 35 34 33 32 31 65 1190K 179,2K 37.31K 10.00K 3270 1255 115 547.3 145 265.1 3 2 HHK 169.3K 35.57 K 9605 3160 1218 116 533.4 146 259,2 63 1037K 160,0K 33.93K 9227 3054 87 147 253.4 247.8 1183 519.9 62 968.4K 151,2K 32.37 K 2952 2854 8867 88 89 1149 118 506.8 148 61 904.9 K 143.0K 30.89 K 8523 1116 119 494.1 149 242.3 +30 31 32 33 34 35 36 37 +150 237.0 -60 29.49 K 28.15 K 845.9K ---30 29 135,2K 127,9K 8194 +60 61 62 63 +120 121 2760 +90 1084 481.8 59 791.1K 7880 7579 2669 91 1053 469.8 58 740.2K 28 121 1 K 26.89K 92 93 94 122 123 124 2582 1023 458.2 57 27 26 25 692.8K 114.6K 25.69 K 7291 2497 994.2 446.9 56 55 54 648.8K 108.6K 24.55K 7016 64 65 66 67 68 69 2417 966.3 435.9 607.8K 102.9K 23.46K 6752 2339 95 939.3 125 425.3 24 23 22 97.49K 6 22,43K 6500 569.6K 2264 96 97 913.2 126 414.9 53 534.1 K 92.43K 21.45K 6258 2191 887.9 127 404.9 52 501.0K 87.66K 83.16K 20.52K 38 6026 98 2122 863 4 839 7 128 129 395.1 470.1K 19.63K 5805 +39 2055 385.6

3.3 FUNCTIONAL DESCRIPTION

3.3.1 Memory Organization

The memory is organized into 1024 memory words of 72 bits each (expandable to 96 bits). Each memory word therefore comprises four 18-bit external data words. Figure 4 is a block diagram of the memory organization. The memory stack itself is packaged on eight identical printed wiring, glass-epoxy substrates, with 128 two-turn word lines on each board, for a total of 1024.

Each word-line wraps twice around 144 plated wires, with the corresponding wires in each of the eight boards connected in series. At the far end, each pair of adjacent wires is shorted together, forming seventy-two pairs, with each pair traversing between all 1024 word-lines. The opposite ends of each pair terminate at the input of a differential sense amplifier. The outputs of a bi-directional digit driver current source is also connected to each pair of wires at the same end as the sense terminations. A specific bit storage location is formed at the crossover points of a particular word line and a pair of plated wires.

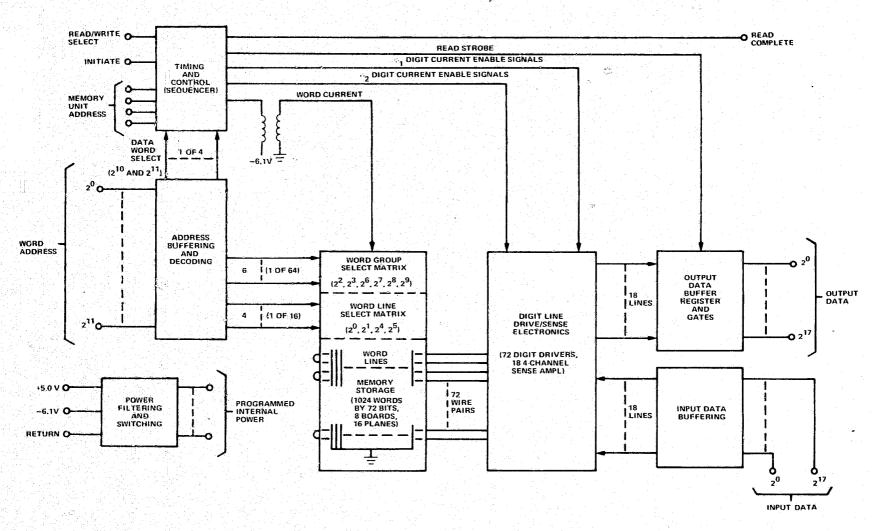
Using two wires for each bit storage (i.e., two crossovers) allows a differential implementation for information sensing, virtually eliminating common-mode noise problems and increasing the signal outputs at any given word current level, thus permitting operation at lower word currents than would have been required with a single crossover-per-bit implementation.

A memory word consists of the 72 bits under a single word line on a particular memory stack board. A particular data word address uniquely locates an 18-bit data word by identifying a word line and a group of 18 sense amplifier channels or 18 digit driver current sources.

The only electronics packaged as part of the memory stack is associated with word line selection. The rest of the electronics is packaged on three similar board assemblies.

3.3.2 Word-Line Selection and Drive

Figures 5 and 6 show the word current selection and drive method. Word-line addressing is accomplished through a two-level tree of transistor switches. The first level steers the word current to one of 64 unique areas of the stack. The second level steers the word current into one of 16 word lines in the particular word group addressed through the first level. Both levels are packaged on the memory stack boards.



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Figure 4. Overall Functional Block Diagram

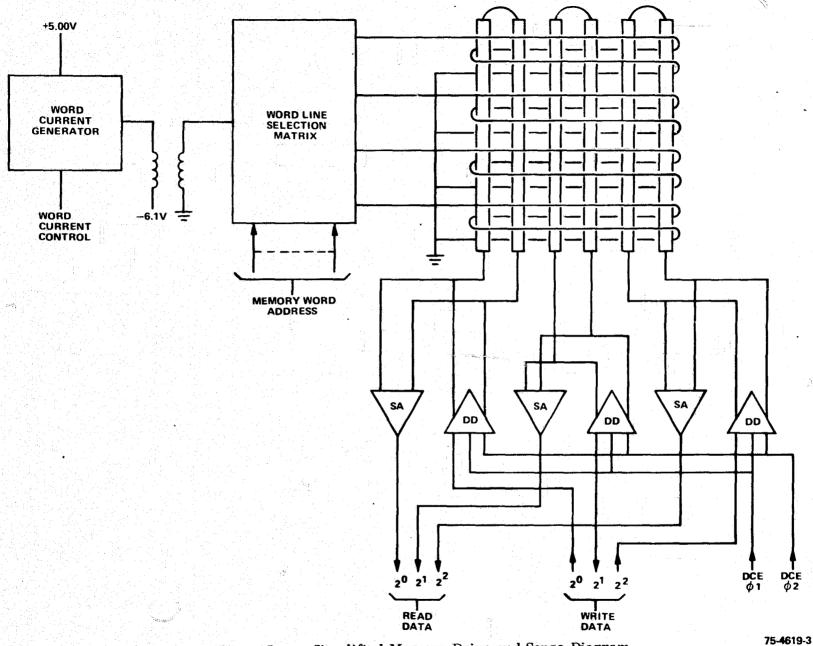


Figure 5. Simplified Memory Drive and Sense Diagram

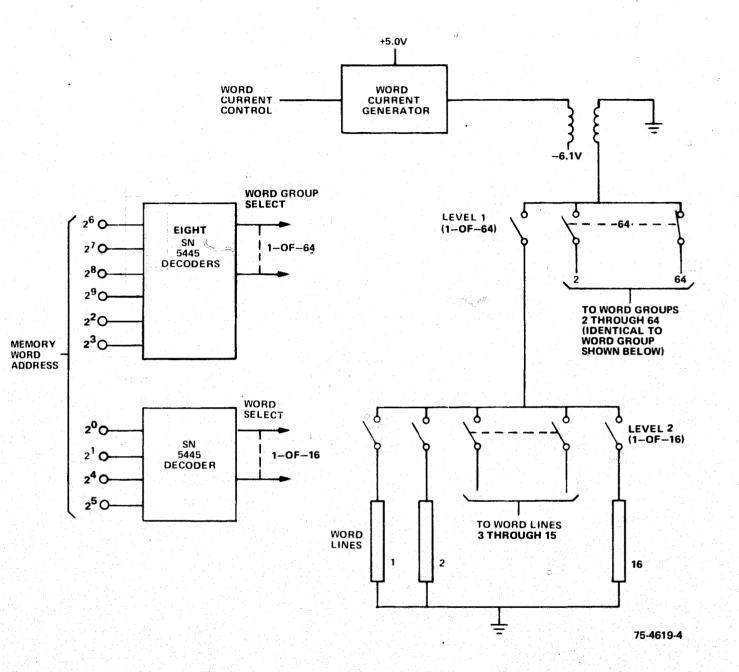


Figure 6. Word-Line Selection Matrix

The data word address is decoded in the sequencer, using SNC 5445 Binary-to-Decimal Decoders. Address bits 2^2 , 2^3 and 2^6 through 2^9 are decoded into 1-of-64 and identify the word group. Bits 2^0 , 2^1 , 2^4 and 2^5 are decoded into 1-of-16 and identify the word line within a group. Bits 2^{10} and 2^{11} identify a particular data word location (1-of-4) along the addressed word line. The apparent anomaly in sequence of the bits allocated for identification of word group and word line is a result of test considerations. With the switching matrix implementation used in the system, the address bit allocation defined above will identify adjacent word lines across a plane when the address sequences in a straight binary code.

Since only one end of each word-line is actively switched (with the opposite end returned to ground) only the addressed word-line has any voltage applied to it (with reference to the quiescent level). Thus, current flow in the stack resulting from charge transfer to/from stray capacitance is minimized and stack charge "restoration" is not necessary. The resulting design is significantly less complex, faster and more noise-free.

A transformer is used for coupling between the word current generator and the word line selection matrix to negate the need for a third, high-voltage power input. The transformer also provides some additional measure of noise reduction.

3.3.3 Control and Sequencing

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The memory design does not use a discrete internal clock. Instead, memory sequences are generated from a series of programmable delays. A diagram of the sequencer logic is shown in Figure 7. Each delay is programmable, independent of any other delay. (The actual programming is accomplished by selection of discrete component values). Thus, timing sequences can be optimized for performance and power consumption.

Power to all but a minimum of control logic is switched off between memory cycles. The delay circuit is designed to come up in a normalized state when power is applied.

When an Initiate signal occurs, the power switch is turned on. If the signal is of longer duration than delay τ_A (approximately 35 nanoseconds), then the Initiate Override signal is actuated, locking the memory in the operate mode until the read or write cycle is completed.

Power to the digit drivers, sense amplifiers, and associated logic is also controlled. through the sequencer. The corresponding power switches are physically located on the digit electronics board assemblies.

Delays $\tau_{\rm B}$ through $\tau_{\rm E}$ are activated for a write cycle. Delays $\tau_{\rm B}$ and $\tau_{\rm D}$ set the width of the two phases of digit current and $\tau_{\rm C}$ sets the separation between the two phases. Delay $\tau_{\rm E}$ controls the duration of the word current. The ϕ_1 and ϕ_2 digit current controls for one of the four possible data words are activated, depending on the states of address bits 2^{10} and 2^{11} .

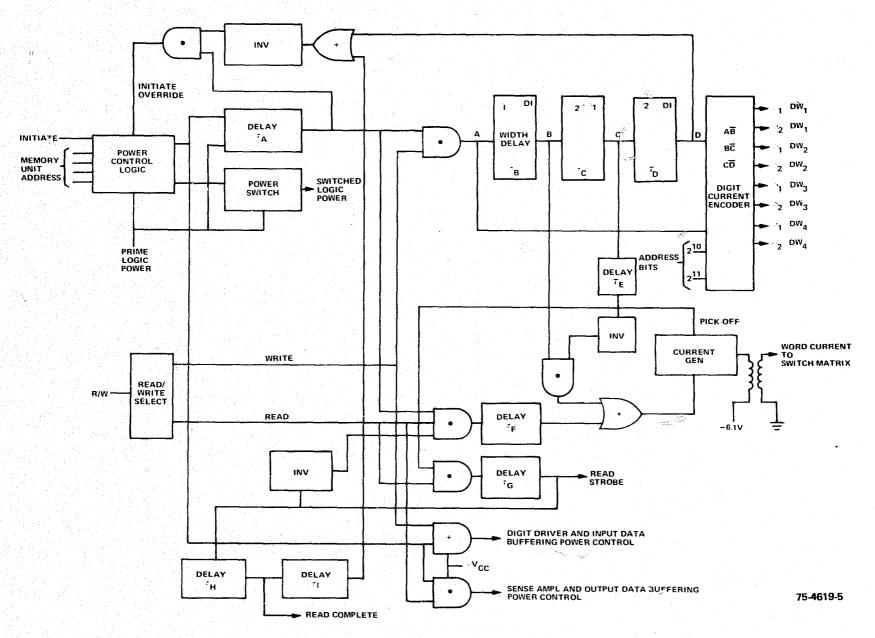


Figure 7. Sequencer, Logic Diagram

Delays ${}^{\tau}_{\rm F}$ through ${}^{\tau}_{\rm I}$ are activated during a read cycle. Delay ${}^{\tau}_{\rm F}$ starts the word current after power start-up transients have had an opportunity to dissipate. A pick-off from the word current level is delayed by ${}^{\tau}_{\rm G}$ and used as the read strobe, which clocks the sense amplifier outputs into the output data buffer register. Delays ${}^{\tau}_{\rm H}$ and ${}^{\tau}_{\rm I}$ set the duration of the read complete and the post-read data hold periods, respectively.

3.3.4 Write Operation

The memory timing for a write cycle is shown in Figure 8. For proper operation, the address, data and read/write control signals must be stable prior to the leading edge of the initiate command and must remain stable until the write cycle has been completed.

When an initiate command pulse occurs in the presence of a low (or ground) level on the read/write control line, power to the sequencer and to the write electronics is turned on. A low impedance path is connected from the word current generator to a particular word line (through the word line selection matrix) as identified by address bits 2^0 through 2^9 . A group of 18 digit driver current sources is then energized for ϕ_1 current. The particular current sources are identified by address bits 2^{10} and 2^{11} . The polarity of current (i.e. direction along the plated wire element) from any current source is controlled by the logic level of the data input to that current source. The ϕ_1 digit current is then terminated and ϕ_2 current enabled. The two phases are of equal amplitude and duration. This balanced current implementation precludes any hysteresis build-up due to an unequal history of data "one" and "zero" writes.

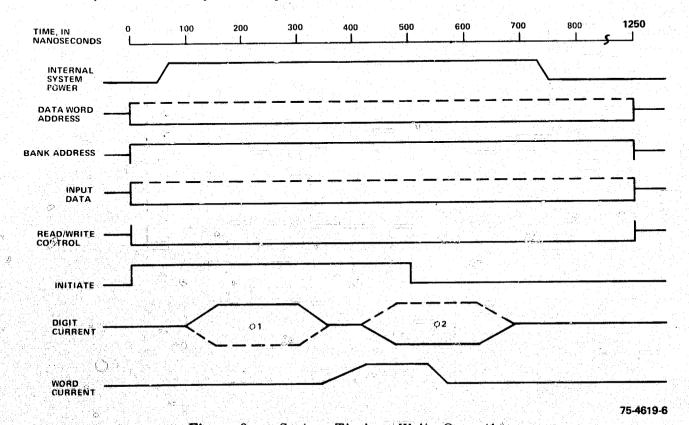


Figure 8. System Timing, Write Operation

The word current generator is energized early enough that the terminating transition of the word current can be made to occur during the time when ϕ_2 digit current is at full amplitude. Data is "written into" the wire when the word current terminates in the presence of digit current.

At the end of the ϕ_2 digit current, the write cycle is complete and internal system power is turned off. A write cycle, from the leading edge of the initiate command to turn-off of system power, requires approximately 750 nanoseconds.

3.3.5 Read Operation

The memory timing for a read cycle is shown in Figure 9. For proper operation, the address and read/write control lines must be stable prior to the leading edge of the initiate command and must remain stable until completion of the read cycle.

When the initiate command pulse occurs in coincidence with a high level on the read/write control line, power to the sequencer and the read electronics is turned on. A low impedance path is again connected to the addressed word line through the word line selection matrix. A group of 18 sense amplifier channels are selected, as identified by address bits 2^{10} and 2^{11} .

After any transients generated in the sense amplifiers have had a chance to settle out, the word current generator is energized. Signals are induced in the plated wires during the word current transients and are amplified by the sense amplifiers. The leading edge transient of the word current is controlled to effect the widest useable "window" in the sense amplifier output. The amplifier outputs are used as steering inputs to buffer storage registers. The polarity depends on the state of the information previously "written into" the plated wire.

The information "read out" during the turn-on transient of the word current is clocked into the the buffer register by the strobe. The strobe is generated by a level detector in the current generator. This minimizes possible uncertainties in strobe position.

The read-complete signal is initiated when the data is plocked into the buffer register. It is maintained for a minimum of 250 nanoseconds and a maximum of 450 nanoseconds. Output data is maintained in the buffer register for at least 150 nanoseconds after termination of the read complete signal. At the end of this time the read cycle is complete and internal power is switched off.

The data and read complete sources are Series 54 open collector logic elements. A low impedance (i.e. output transistor on) denotes the active level for the read complete line and a logic zero on the data lines. The only time the low impedance condition will exist on a data line is during the actual read-out of a bit 0.

3.4 ELECTRICAL PARTS

High-Rel, screened parts were used in construction of the memory. Six pieces of each electronic device were submitted to GSFC for evaluation.

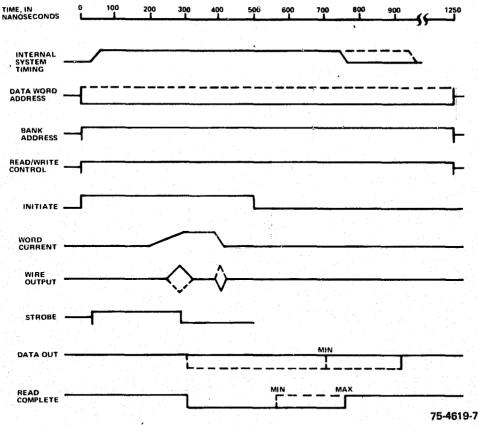


Figure 9. System Timing, Read Operation

3.4.1 Logic Circuits

Series 54 TTL integrated circuit logic elements were used throughout the memory. These were procured per vendor High-Rel specification SNC which is MIL-STD-883, Class B.

3.4.2 Discrete Parts

Two types of established reliability resistors were used in the memory; the RCRXXG Composition and the RNR55C metal film. The RCRXXG were procured to S failure-rate levels and the RNR55C were procured to R failure-rate levels.

Three types of capacitors were used; the CSR 13 style established reliability tantalum with failure rate of R or lower, the CKRO6 style, established reliability ceramic with failure rate of R or lower, and the CM series cap per MIL-C-5/18 with additional screening. Transistors and diodes were either purchased as JAN TX parts or screened to JAN TX equivalent per the documents indicated in the parts control list.

3.4.3 Transformer

A single rf transformer was used in the memory for coupling the word current from the generator to the memory stack. The transformer was fabricated in-house to the requirements of MIL-C-15305, Type LT6K, with temperature cycling per MIL-STD-202, Method 102. Condition C, except 10 cycles at -55°C.

3.4.4 Sense Amplifier

The four-channel sense amplifier (SC 12200 FB2) is shown in Figure 10. The input terminating resistors are external to the package.

3.4.5 Hybrid Circuits

Six different hybrids are used in the memory. These are custom circuits manufactured in-house and screened to meet the requirements of this program. Each of these circuits is described briefly in the following paragraphs.

3.4.5.1 Delay Circuit

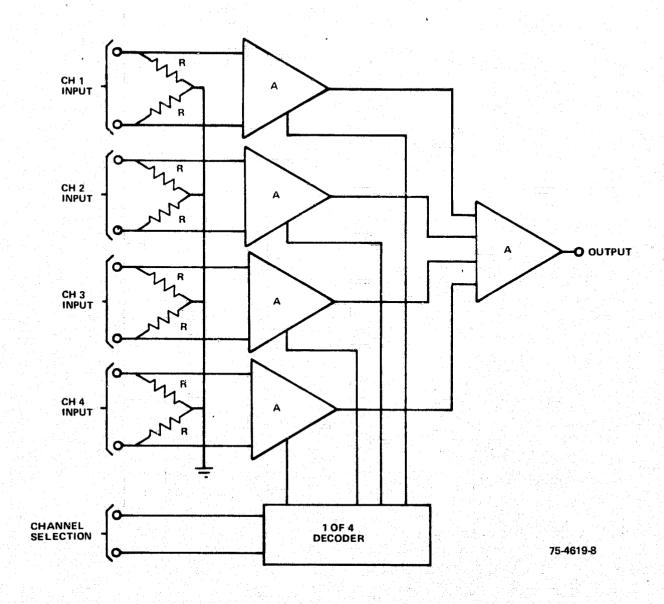
The delay circuit is shown, functionally, in Figure 11. Only the high-to-low transition at the input is delayed at the output, with both the true and complement outputs available. The delay is adjustable from a minimum of approximately 25 nanoseconds to a maximum of several microseconds.

3.4.5.2 Word-Line Selection Circuits

The word-line selection circuits are shown in Figures 12 and 13. A particular switch is closed by grounding the corresponding selection input. The first and second level switches are packaged together. A particular package contains one first level switch and two banks of four second level switches each. Each of four second level selection inputs controls one switch in each bank. A single selection input controls the first level switch. The pin-outs are configured so that a first level switch can be connected to a second level bank in a different package, as well as to a bank in its own package.

3.4.5.3 Digit Driver

The digit driver is shown in Figure 14. Basically, it consists of two current sources with steering such that, depending on the logic inputs, one of the sources may be enabled to conduct current through the load in a particular direction. The T1 and T2 inputs denote successive time periods for the two opposite phases of digit current. The D and \overline{D} inputs denote the true and complement levels of an input data bit. If D is true, then current will flow in the direction indicated during T1 and in the opposite direction during T2. The current flow would be opposite if \overline{D} were true.



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Figure 10. Four-Channel Sense Amplifier, Functional Diagram

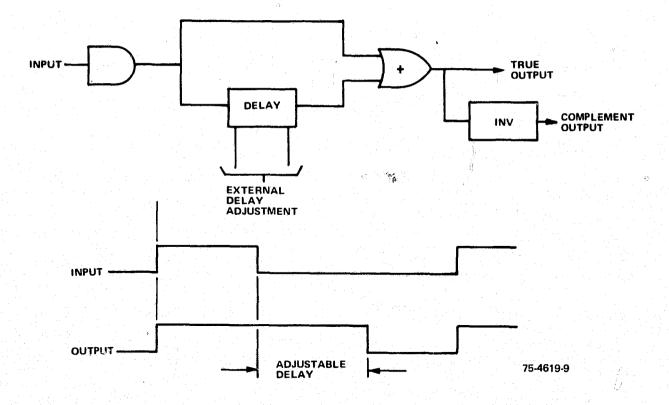


Figure 11. Delay Circuit, Functional Diagram

3.4.5.4 Power Switches

Two types of power switches are used in the memory. One type provides two independently controlled logic level (i.e., +5.0 V) outputs from the primary +5 V input. The other type provides two sets of +5.0 V and -6.1 V outputs from the corresponding inputs. Each set is controlled independently. The switches themselves consume no power when in the OFF state. The switches perform no regulation. They are shown functionally in Figures 15 and 16.

3.5 MECHANICAL DESIGN

3.5.1 Stack Design

The plated wire memory stack used in the LP RASM used a standard Motorola plane design for spaceborne memories developed to high reliability, quality assurance, and workmanship standards. The primary design goal of the stack was simplicity of fabrication combined with high reliability. The number of solder joints and plated through holes are minimized to accomplish this end. The stack consists of eight planes arranged and interconnected to meet the specific requirements of the LP RASM. Specific details of stack construction are described below.

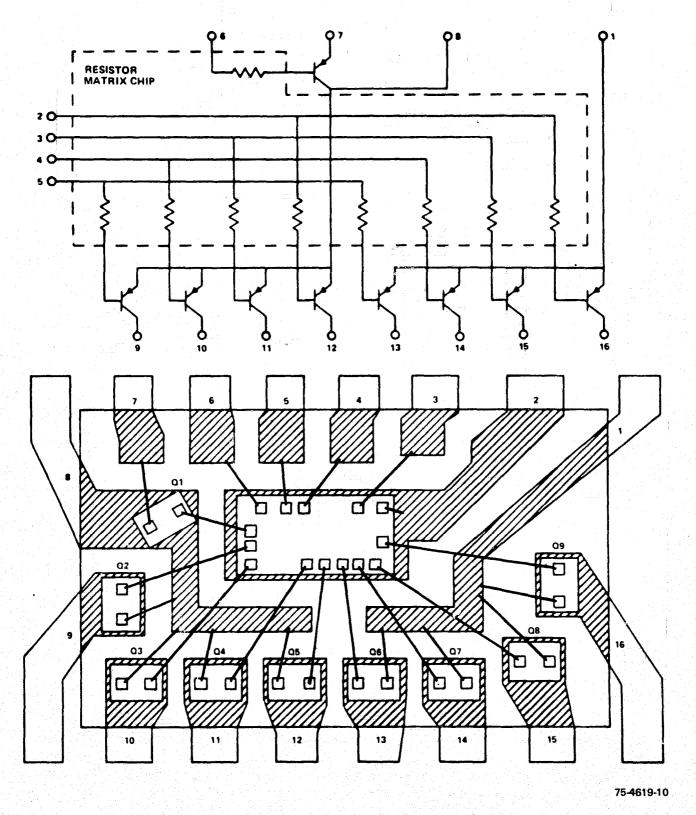


Figure 12. Custom Package and Layout

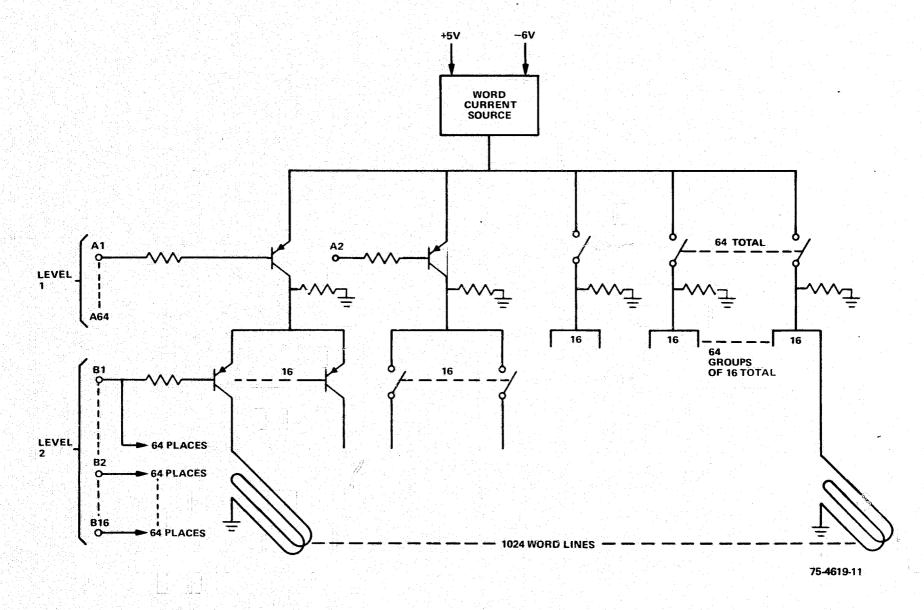


Figure 13. Word-Line Selection Matrix, Functional Diagram

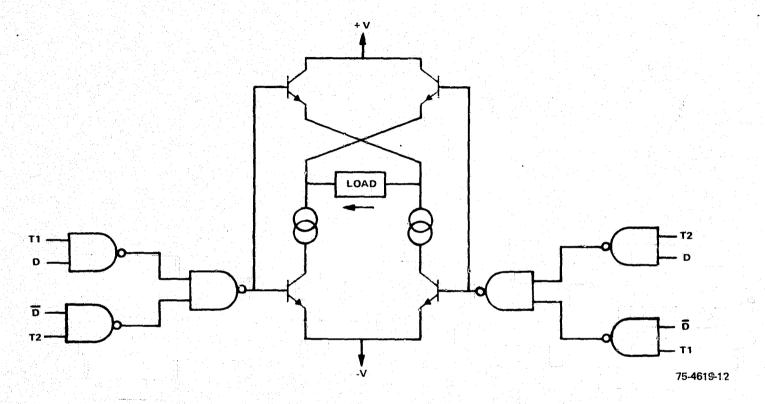


Figure 14. Digit Driver, Functional Diagram

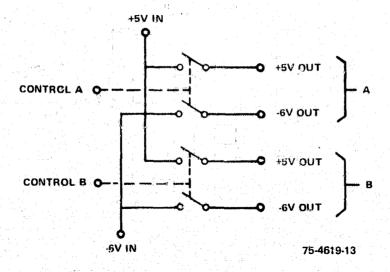


Figure 15. Power Switch +5V/-6V

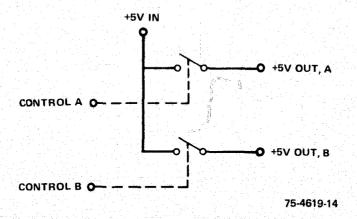


Figure 13. Power Switch +5V/+5V

The tunnel structure, the heart of the memory plane, contains the word lines and the plated wire which stores the bits of data. The plated wires are installed in 0.007 diameter tunnels on 0.025 centers in a polymide-FEP tunnel matt. The tunnel matt is constructed by forming the FEP (between the polyimide film) around dummy wires at controlled temperature, pressure and wire tension. After complete assembly processing the dummy wires are removed and the plated wire is installed in the tunnel.

Word lines of etched copper on glass epoxy board are laminated to each side of the tunnel matt so that they are perpendicular to the tunnels (plated wire). The word lines are double turn (twice around the wires per line). Their mechanical configuration is 0.010 wide conductor, an intervening 0.005 space and another 0.010 conductor, all on repetitive 0.050 centers. Plated-thru holes at each end of the tunnel matt creates the double turn word lines.

Each carrier structure contains 64 word lines and 100 bit lines (Plated wire tunnel pairs). To provide the desired storage capacity for the LP RASM only 72 tunnel pairs are populated (plated wire installed).

Keepers, of high magnetic permeability and processed with extreme care, are bonded to the outer surface of the glass epoxy board which support the word lines to contain the word line field and shield against external magnetic fields. The tunnel matt and word lines are carefully fabricated and then laminated into a subassembly using multilayer printed wiring board techniques. The keepers are then laminated using similar techniques. A cross section of the tunnel structure is shown in Figure 17.

The memory plane is fabricated by laminating two tunnel structures to each side of a motherboard. The motherboard is a two-sided printed wiring board which has a ground plane laminated in the center. The input and return for the matrix is tracked to the edge of the board where pc board interconnect is used to interface with the plane. Two tunnel structures per plane provide 128 word x 72 bit capacity. Installation of the 8 word-drive flat packs per side, by lap soldering, completes the memory plane subassembly. Memory plane construction is shown in Figure 18.

The memory stack consists of eight memory planes electrically and mechanically integrated into one unit to provide 1024 words x 72 bits of storage. The digit lines of each plane are interconnected with flat flexible circuitry bonded to the motherboard which permits the stack to be opened as necessary during assembly and rework. The plated wire is formed like a "hairpin" and installed into the top and bottom carrier structure (similar to a trombone slide). The two ends of the plated wire are lap soldered directly to the conductor of the interconnecting flex cable. This approach for installing the plated wire minimizes the number of solder joints required while providing the required stress relief.

PC board interconnect with miniature connectors (see Figure 2) is used to interconnect common word drive signals from plane to plane and carry all digit and word signals to the electronics. The use of printed circuitry interconnect provides controlled impedance and line characteristics. The connectors allow the stack to be connected/disconnected from the electronics with minimum effort.

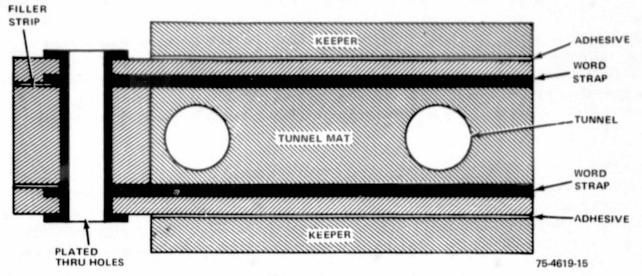


Figure 17. Tunnel Structure Construction

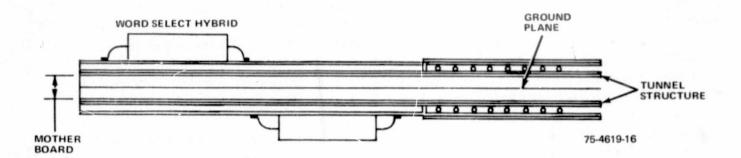


Figure 18. Memory Plane Construction

During assembly, spacers are installed at each tie-down location on the planes to precisely position the planes relative to each other in the stack. The tie-downs are located to provide maximum stability under dynamic conditions.

3.5.2 System Packaging

The 4k x 18 bit Low Power Random Access Spacecraft Memory developed by Motorola consisted of a 1k by 72 plated wire stack, two digit drive/sense electronics boards and a timing/control/word drive board, all contained in an aluminum or magnesium housing.

The concept of stacking the electronics boards in the same manner as the planes was used in the complete memory package. The timing/control/word drive board is located on top of the plated wire stack while the two digit drive/sense boards are located below the plated wire stack. This arrangement eliminates interference between signals as the digit line interconnects leave the plated wire stack in one direction while the word lines go the other direction.

The size of the memory plane (i.e., number of word lines, digit lines, required structural mounting and word drive matrix area) determine the "plan view" size of the system package. The basic plane size is 8.05" long x 4.38" wide and contains 8 tie-down screws. The electronics boards have the same mounting tie-down locations and length as the plane but are 5.0" wide.

Mechanically, each of the electronic boards are essentially identical. Each consists of a printed wiring board to which flat pack integrated circuits (Motorola plated wire hybrids or conventional logic) are lap soldered and a few discrete components are mounted. The digit boards contain the digit drivers, sense amplifiers, data input buffers and data output registers. The third board contains the timing and control logic and the transistor word drive select electronics.

After the boards are assembled, a thin conformal coating is applied to the board assembly. This coating provides protection in a high humidity environment, protection against shorting across components and a vibration damping effect on the boards. This provides an encapsulated assembly that is easily disassembled for servicing or repair.

Flat flexible cable is used for interconnecting between board assemblies. The flex interconnect is arranged so the plated wire stack and printed wiring boards can be assembled in the system stack (described previously) or opened out to provide access for testing or troubleshooting of the boards, the stack or the system. The connection to the external connector is a conventional hard wire harness.

The plated wire stack and electronics boards are assembled by stacking them into a single unit and installing them in a housing. Spacers are provided between the boards and the stack at the tie down locations to position them with respect to each other. Eight special high-strength screws pass through the spacers and secure the system in the housing.

The system assembly is contained in a single protective housing which was machined from AZ 31B magnesium material and shipped to GSFC for gold plating. The memory housing is 8.6" long x 6.3" wide x 2.9" high (exclusive of mounting flanges and connectors) establishing a volume of 157 cubic inches. The system has a total weight of 5.80 pounds.

3.5.3 Materials

Motorola's basic memory system design uses materials that meet the requirements of high reliability spaceborne hardware, particularly in the area of environment, outgassing and compatibility with other materials in the spacecraft. Materials are used that were approved on the Mariner '71 subsystems which Motorola designed and fabricated and have since been proven by the success of the mission. These materials were also used on the two memories previously delivered to GSFC under contract No. NAS 5-23163 with the exception of an adhesive used in the fabrication of the memory planes which was changed to facilitate manufacturing. This adhesive has been tested and approved for use by GSFC.

SECTION 4

TESTING

4. GENERAL

Comprehensive testing was performed on the memory and its subassemblies at each level of assembly.

4.1 SYSTEM LEVEL TESTING

Acceptance tests were conducted at the system level. Acceptance testing included complete functional tests at temperature extremes of +85°C and -40°C. The acceptance test procedure and test data records are included as an Appendix, Acceptance ambient temperature functional tests were repeated after environmental testing.

Environmental testing consisted of both sine and random vibration, shock, and vacuum (to 10^{-5} mm Hg). The memory unit was continuously exercised with a worst case pattern during all environmental testing.

4.2 MEMORY STACK TESTING

A 100 percent on-line test was performed on the plated-wire during manufacture under relatively severe test patterns and word/digit current variations.

In addition to the on-line wire test, the memory stack was subjected to comprehensive worst case test patterns at the stack level using an EH 8500 computer controlled stack tester. Tests performed include adverse history being hard written in 1000 times and then the opposite polarity being written one time and immediately read out. Also adjacent bits are written into 10,000 times at the opposite polarity of the bit under test and then the bit under test is read out to test the effects of adjacent bit disturbs.

Any wire which did not meet the minimum output level requirements was replaced and the unit retested.

4.3 HYBRID CIRCUIT SCREENING

All hybrid microcircuits used in the memory were subjected to extensive, 100-percent screening to criteria based on MIL-STD-883 criteria. In addition to comprehensive electrical tests at temperature extremes, these tests included pre-cap visual inspection, centrifuge, operational vibration, stabilization bake, thermal cycling, power aging, and leak testing.

ATTACHMENT I

ACCEPTANCE TEST PROCEDURES

LOW POWER RANDOM ACCESS

SPACECRAFT MEMORY

PART NO. 01-P13701D

(35 PAGES)

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SCOPE

This procedure and the test data sheet (12-P11216B) define the unit acceptance requirements for the Low Power Random Access Spacecraft Memory, Motorola Part No. 01-P13701D, manufactured under Contract No. NAS 5-23163.

REFERENCE INFORMATION 2.

SPECIFICATIONS APPLICABLE 2.1

S-562-P-24

Low Power Random Access Spacecraft

Memory.

12-P13721D

Test Data Record

12-P11173B

Motorola Plated Wire Memory Tester

Operating Manual.

DEFINITIONS

1

UP position on DATA and ADDRESS

switches. DATA and ADDRESS lamps ON

DOWN position on DATA and ADDRESS

switches. DATA and ADDRESS lamps

OFF

Tester

Motorola Plated Wire Memory Tester

MSB

Most Significant Bit

LSB

Least Significant Bit

Error Lamps

Lamp ON indicates ERROR present.

MOTOROLA INC. Government Electronics Division

CODE IDENT NO. DWG NO.

SIZE

94990

12-P13722D

8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

SCALE

REVISION

SHEET 3

TEST EQUIPMENT AND ENVIRONMENTAL REQUIREMENTS

3.1 TEST EQUIPMENT

3.

The calibrated test equipment listed below, or its equivalent, will be required to perform this test procedure. Any equipment used as an equivalent to that listed below shall be recorded in the data sheet.

STANDARD TEST EQUIPMENT

TTEM		ANUFACTURER!S	
DC Milliammeter	Hewlett Packard	428 B	0-10 Amp.
Oscilloscope	Tektronix	585	50ns/cm
Scope Plug-In	Tektronix	82	Tr 1.5ns
Digital Voltmeter	Hewlett-Packard	3440A	Accuracy ± .05% of reading
Counter	CMC	727BN	0.1% <u>+</u> 1/2 LSB
DC Multifunction Unit	Hewlett-Packard	3444A	0-999.9 ma. 0-9.999 megohms
Oven	Wyle	CO-106-1800	-100°F to +500°F
Power Supplies	Precision Design Inc	5015-A	0-50V, 1.5 Amp.
Power Supplies	Precision Design Inc	5015-S	0-50V, 1.5 Amp.
Pulse Generator	CH	139B	10Hz to 50MHz

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AV-2-B-199H-100A-3/69 DWG FORMAT

NON-STANDARD TEST EQUIPMENT

(NO CALIBRATION REQUIRED)

Motorola Plated Wire Memory Tester 01-Pl1170B001

NOTE:

The Motorola Plated Wire Memory Tester supplies inputs to the memory under test from SN5400 series logic and presents a single unit load of SN5400 logic on the memory output lines.

Motorola Tester Interface Box T-5909

NOTE:

The Interface Box puts a 51 ohm resistor in series with all of the signals going to the memory and provides a 1K pull up resistor to signals coming back from the memory.

ENVIRONMENTAL TEST EQUIPMENT

ITEM	MANUFACI	MODEL NO.		
Vibration Tester	LING		27 5	
Vacuum Chamber	NRC		2707	
Shock Tester	MRL		2424	
Vibration Test Fixture	MOT			

3.2 TEST CONDITIONS

Unless otherwise specified all tests shall be performed under the following conditions.

3.2.1 Power Supply Voltage

The unit specified to be tested shall operate from the following

DC source voltages: +5.0V ± 5% -6.1V + 5%

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8201 E. McDOWELL ROAD				
Government Electronics Division	A	94990	12-P137221	
MOTOROLA INC.	SIZE	CODE IDENT NO.	DWG NO.	

3.2.2 Ambient Temperature

The unit shall be tested in a laboratory area having a temperature of $+25 \pm 10^{\circ}$ C (77 $\pm 18^{\circ}$ F).

3.2.3 Ambient Humidity

Normal laboratory ambient, not to exceed 90%.

3.2.4 Ambient Atmospheric Pressure

Normal laboratory ambient.

3.2.5 Stabilization Period

The test equipment shall not be used to conduct tests until after a minimum warm-up period of 15 minutes.

4. TEST SCHEDULE

The testing to be performed on each memory unit is as follows:

- 1. Physical Characteristics (Weight and Dimensions)
- 2. Comprehensive Initial Functional Tests.
- 3. Operational Tests at Temperature Extremes.
- 4. Operational Vacuum Tests
- 5. Operational Vibration Tests
- 6. Operational Shock Tests
- 7. Final Functional Tests

Tests 3 through 6 may be performed in any sequence.

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TEST RECORDS

5.1 TEST LOG

The Test Log shall be used to record the history of the memory, starting from the first system test. The log shall reference all testing, rework and idle time for the particular memory unit.

5.2 DATA RECORD

All test results shall be recorded in the Test Data Record, Motorola Document No. 12-P13721D.

- 6. PHYSICAL CHARACTERISTICS
- 6.1 WEIGHT

Place the LP RASM on the scale and read and record, in the data sheet, the weight of the memory, in pounds.

6.2 DIMENSIONS

Measure and record, in the data sheet, the outside dimensions as shown in Figure 1. Compute and record, in the data sheet, the memory volume by multiplying dimension W by dimension H by dimension D. (V = W X H X D).

- 7. INITIAL FUNCTIONAL TESTS
- 7.1 INTERCONNECTION

Record connector mate/demate history according to IUE connector log requirements.

At the Interface Box, set memory power to OFF. Connect the unit under test as shown in Figure 2, except that the Interface Box will not be connected to the Plated Wire Memory Tester. The

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connections are all labeled on the Interface Box.

Turn the coarse voltage controls fully counterclockwise and turn on power to all electrical test equipment.

Using the scope, adjust the Pulse Generator for $+3 \pm 0.1$ V positive pulses of 450 ± 10 nanosecond duration (at the 50 percent points) at a 500 ± 1.0 KHz rep rate. (Use the counter to adjust the rep rate). The pulse generator output must be terminated in 50 ohms and connected to the tester when making these adjustments.

Normal precaution shall be taken to ensure that the equipment is not dropped or damaged in any way while it is being handled, or while the connectors are being engaged.

7.2 PRELIMINARY CONTROL SETTINGS

Set the Tester and Interface Box controls as follows and maintain these control settings unless otherwise directed in the individual tests.

CONTROL	<u>2</u>	ETTING	
TESTER			
BD1-BD4(24 Switches)		Jp	
Tape Reader Power		ight Of	f
Run-Off-Rewind Switch		FF	
Tester Power		ight On	
Address Switches	I	own	

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CONTROL

SETT ING

TESTER (Cont.)

Data Switches

UP

READ/WRITE

WRITE

Word Length

24

READ 1/ READ 7 Switch

READ 1

Address Pattern

SEQ.

Data Pattern

MAN

Frequency

EXT.

INTERFACE BOX

Memory Select Switches

A11 2.4V

Input Current Switch

GND

Output Pullup Resistor

GND

WC Switch

OFF

Initiate Pulse Switch

GND

WC2 Switch

OFF

Memory Power

OFF

7.3 INITIAL POWER SUPPLY CONDITIONS

Using the DVM, adjust the three supplies as follows:

+5V to Interface Box: $+5.0V \pm 0.1V$

+5V to Memory: +5.0 + 0.1V

-6.1V to Memory: $-6.1 \pm 0.1V$

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Set the meter selection switches to measure current and leave them in this position. Disconnect the output side of all three power supplies from the Interface Box.

All subsequent mention of +5V in the procedure refers to memory power unless otherwise specified.

- 7.4 CHASSIS ISOLATION
 - Using the digital ohmmeter verify that the impedance between the memory chassis and ground test point on the interface box is > 9 megohoms. Record the results in the Data Sheet.
- 7.5 INPUT SIGNAL LOADING
- 7.5.1 Connect the two +5V supplies to the Interface Box. (If the Interface Box supply overloads, reset it by turning its power off and back on).
- 7.5.2 Remove the jumper wire from the INT PULSE test point. Connect the digital ammeter between the INT PULSE and INT PULSE SW test points. Momentarily turn the MEMORY POWER switch to ON and measure and record the current. Set the INT PULSE switch to the +2.4V position. Momentarily set the memory power switch to ON and again measure and record the current. Disconnect the ammeter and connect the jumper wire between the INT PULSE and INT PULSE SW test points.
- 7.5.3 Replace the jumper from the MEMORY SELECT 1 test point to the MEMORY SELECT 1 SWITCH test point with the digital ammeter.

 Momentarily set MEMORY POWER to ON and measure and record the current. Set the MEMORY SELECT 1 SWITCH to the GND position.

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Momentarily set MEMORY POWER to ON and measure and record the current.

Disconnect the ammeter and replace the jumper wire. Set the MEMORY SEVECT 1 SWITCH back to the +2.4V position.

- 7.5.4 Repeat paragraph 7.5.3 for MEMORY SELECT 2, MEMORY SELECT 3, and MEMORY SELECT 4.
- 7.5.5 Connect the ammeter from the READ/WRITE test point to the INPUT CURRENT SWITCH test point. Set the Initiate Pulse Switch to 2.4V. Momentarily set the memory power switch to ON. Measure and record the current. Move the INPUT CURRENT SWITCH to the +2.4V position. Momentarily set the MEMORY POWER switch to ON and measure and record the current. Return the INPUT CURRENT SWITCH to the GND position.
- 7.5.6 Connect the ammeter between the ADDRESS BIT 2° and the INPUT CUR-RENT test points. Momentarily set the MEMORY POWER switch to the ON position and measure and record the current.

Set the INPUT CURRENT SWITCH to the +2.4V position. Momentarily set the MEMORY POWER switch to the ON position and measure and record the current. Set the INPUT CURRENT SWITCH back to the GND position.

Repeat the above two measurements at each of the 12 address bit test points. Connect a jumper between the R/W and GND test points. Repeat the above two measurements at each of the 18 DI test points (i.e. with the ammeter conn. between a DI test point and the INPUT CURRENT test point).

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Verify that the MEMORY POWER switch is OFF. Remove the jumper from the R/W test point and install the jumper from the INT PULSE test point back in its original position.

- 7.6 VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS.
- 7.6.1 Connect the Interface Box to the tester. Connect the -6.1V power supply to the Interface Box. At the tester, depress the STOP and RESET pushbuttons. Set the initiate pulse SW to pulse position.
- 7.6.2 Turn the MEMORY POWER switch ON and push the START button on the tester. The tester will write a "1" in all data bits in all 4096 addresses one time and stop.
- 7.6.3 Set the READ/WRITE switch on the tester to the READ position.

 Push the tester START button. Using the Dual Trace of the oscilloscope, measure and record in the data sheet the voltage at the READ COMPLETE test point 150 ns after the leading edge of the pulse at the INITIATE PULSE test point. The voltage shall be ≤100 mv. Disregard errors.

(The read complete output for this test and the data outputs for the next test are terminated with a 1K resistor to GND).

7.6.4 Measure and record in the data sheet the voltage at each of the 18 data output lines that occurs 500 ns after the leading edge of the Initiate Pulse. The voltage shall be ≤100 mv. Push the tester stop button. Set the OUTPUT PULLUP RESISTOR switch to the +5V position.

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- 7.7 POWER CONSUMPTION
- 7.7.1 Using the DVM, adjust the $\pm 5V$ and $\pm 6.1V$ memory power supplies to $\pm 5.0 \pm 0.1V$ and $\pm 6.1 \pm 0.1V$, respectively. Record the voltages.

Using the 428B milliammeter, measure and record the current from the +5V memory supply. Compute and record the +5V power.

- 7.7.2 Using the milliammeter, measure and record the current to the -6.1V supply. Compute and record the -6.1V power.
- 7.7.3 Compute and record the total Memory Idle Power.
- 7.7.4 Set the DATA PATTERN switch to SEQ. and momentarily depress the RESET and START buttons. The tester should be cycling through memory addresses.
- 7.7.5 Repeat 7.7.1.
- 7.7.6 Repeat 7.7.2.
 - 7.7.7 Compute and Record the Total Active Power. Momentarily depress the tester stop pushbutton.
 - 7.8 READ COMPLETE TIMING
 - 7.8.1 Connect the oscilloscope as follows; trigger input jack to the INITIATE PULSE test point, channel A voltage probe to the INITIATE PULSE test point and the channel B voltage probe to the READ COMPLETE test point.
 - 7.8.2 Set the DATA PATTERN switch to MAN, READ/WRITE switch to READ, and tester BD1 switch 0 to the up position.
 - 7.8.3 Depress and release the RESET button, then the START button.
 - 7.8.4 Synchronize the oscilloscope on the leading edge of the initiate pulse.

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- 7.8.5 The read complete pulse shall be a negative pulse and shall be generated 500 nanoseconds maximum after the leading edge of the initiate pulse and the duration shall be 250 ns minimum and 450 ns maximum. (All timing relationships shall be measured at the 50% points). Record the pulse delay and duration in the data sheet.
- 7.8.6 Momentarily depress the STOP button and set the READ/WRITE switch to WRITE. Set all data switches to the down position. Depress and release the RESET button, then the START button. Set the READ/WRITE switch to READ and momentarily depress the START switch.
- 7.8.7 Connect the scope channel A voltage probe to the first data output line test point (DO-0). The high-to-low transition on the data output line shall occur prior to (or in coincidence with) the leading edge of the read complete pulse. The low-to-high transition of the data output line shall occur no earlier than 150 nanoseconds following the trailing edge of the read complete pulse. (All timing relationships shall be measured at the 50 percent points).

 Record the results.
- 7.8.8 Repeat the measurements of 7.8.7 at each of the remaining

 17 data output line test points. Record the results.

 Depress and release the stop button.

 7.9 SYSTEM FUNCTIONAL TESTS
- 7.9.1 Depréss and release the RESET button. Set the ADDRESS PATTERN switch to SEQ. Adjust the pulse generator frequency to $600 \pm 1.0 \text{ KHz}$.

Set the DATA PATTERN switch to SEQ.

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7.9.2 Depress and release the START button. The tester will then begin cycling through all memory locations. It steps to the first address, writes a "0", reads a "0", writes a "1" and reads a "1" in all bits in that address word, then steps to the next address, etc. The tester continues this cycle unless an error occurs. Test for 2 minutes and record any errors. Depress the STOP button. Set the READ 1/READ 7 Switch to the READ 7 position. 7.9.3 READ 7 mode causes the tester to write a "0", read a "0" seven times, write a "l", and read a "l" seven times in each memory location. 7.2.4 Depress and release the START button. The Tester will continue to cycle unless an error occurs. Test for 2 minutes and record any errors. 7,9,5 Depress and release the STOP button. Set the DATA PATTERN switch to MAN and the READ/WRITE switch to WRITE. DATA switches to the DOWN position. 7.9.6 Depress and release the RESET button and then the START

7.9.7 Set all DATA switches to the UP position.

button.

7.9.8 Depress and release the RESET button and then the START button.

7.9.9 Set the READ/WRITE switch to READ. Depress and release the RESET button.

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- 7.9.10 Depress and release the START button. Test for one minute.

 Record any errors.
- 7.9.11 Depress and release the STOP button.
- 7.9.12 Set the READ/WRITE switch to WRITE.
- 7.9.13 Set all DATA switches to the DOWN position. Depress and release the RESET button.
- 7.9.14 Depress and release the START button. The memory will cycle thru all 4096 addresses one time and stop.
- 7.9.15 Set the READ/WRITE switch to READ. Depress and release the RESET button.
- 7.9.16 Depress and release the START button. Run for one minute. Record any errors.
- 7.9.17 Depress and release the STOP button.

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- 7.10 RANDOM ACCESS CAPABILITY
- 7.10.1 Set the READ/WRITE switch to WRITE and the ADDRESS PATTERN switch to MAN.
- 7.10.2 Select an address at random with the ADDRESS switches.
- 7.10.3 Set the DATA switches in a random pattern. Depress and release the RESET button.
- 7.10.4 Depress and release the START button. The selected data will be written into the selected address.
- 7.10.5 Depress and release the Stop button. Set the READ/WRITE switch to READ.
 - 7.10.6 Depress and release the START button. The data in this address location will be read out. If an error occurs, note this in the data sheet.
 - 7.10.7 The operator should select 3 other addresses at random, repeating steps 7.10.2 through 7.10.6 to verify the random access capability.
 - 7.11 NON-VOLATILITY TEST
 - 7.11.1 Set the ADDRESS PATTERN switch to SEQ and the DATA PATTERN switch to MAN.
 - 7.11.2 Set the DATA switches to a random pattern. Depress and release the RESET button. Set the READ/WRITE switch to WRITE.
 - 7.11.3 Depress and release the START button. The tester will run through all 4096 addresses one time and then stop. Set the READ/WRITE switch to READ.
 - 7.11.4 Turn memory power to OFF.

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- 7.11.5 Depress and release the RESET button.
- 7.11.6 Turn memory power to ON.
- 7.11.7 Depress and release the START button. If any errors occur, record them on the data sheet. If no errors occur, no words were disturbed when the power was interrupted.
- 7.11.8 Depress and release the STOP button.
- 7.11.9 Repeat 7.11.4 through 7.11.8 four times. Record any errors.
- 7.12 MEMORY SELECT TEST
- 7.12.1 Set the ADDRESS PATTERN switch to SEQ and the DATA PATTERN switch to SEQ. Set the No. 0 switch on BD1 to the down position.
- 7.12.2 Sot the MEMORY SELECT switches to 0000.
- 7.12.3 Depress and release the RESET button, then the START button.

 The tester should indicate an error at the first address.

 Record this address on the data sheet.
- 7.12.4 Repeat 7.12.3 with the memory select switches set to 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, and 1110.
- 7.12.5 Set the MEMORY SELECT switches to 1111.
- 7.12.6 Set the No. 0 switch on BD1 to the UP position. Depress and release the RESET button, then the START button. Allow the tester to run for 2 minutes. Record any errors. Depress and release the STOP button.

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- 7.13 WORST CASE PATTERN TEST
- 7.13.1 Set the DATA PATTERN switch and the ADDRESS PATTERN switch to WCl. Turn the WC switch ON. Depress and release the STOP and RESET buttons.
- 7.13.2 Depross and release the START button. The tester will execute the following sequence:
 - A. Write a "1" in every bit of every word 210 times.
 - B. Write a "0" once in every bit of every word under an even numbered word line in the stack.
 - C. Write a "1" in every bit of every word under an odd numbered word line and read the previously written "0" in every bit of every word under an even numbered word line until the operator sequences to the next group or until an error is detected. The READ light is lit during this cycle.
 - NOTE: If any error lights are ON when cycle C starts, disregard them and depress RESET one time prior to starting the one minute count. This applies to all worstcase pattern tests.

Run in cycle C for two minutes. Record any errors on the data sheet.

7.13.3 Press and release the WCl SEQ button. The tester will execute the preceeding sequence, except "even" and "odd" are interchanged. The WC2 and WC2 lights will indicate the second WCl group is under test. Record any errors.

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- 7.13.4 Repeat 7.13.3 for WC1 groups 3 and 4 in which "1" and "0" are interchanged. Record any errors on the data sheet.

 Depress and release the STOP button. Turn the MEMORY POWER to OFF.
- 8. TEMPERATURE TEST

The temperature tests shall be conducted under normal laboratory conditions, with the exception of temperature.

8.1 TEST SETUP

Place the unit in the temperature chamber a

Place the unit in the temperature chamber and establish the test setup as shown in Figure 3.

- 8.2 LOW TEMPERATURE

 Place the memory unit in a plastic bag and seal the chamber.
- 8.2.1 Decrease the chamber ambient temperature to $-40^{\circ} \pm 3^{\circ}$ C.

 When the chamber has reached this temperature, note the time.
- Beginning 150 minutes after the chamber temperature has reached -40°C, measure and record the thermistor resistance at 10 minute intervals. At each measurement, except the first one, calculate the percent change from the previous reading. When the change is less than 5 percent turn off the chamber and proceed to paragraph 8.2.3.
- 8.2.3 Depress the START button. The memory shall run without error for 2 minutes. Depress the STOP button and record the results.

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- and the -6.1V supply to -6.40 ± .02V. Measure and record the power supply volt and the standby power (paragraphs 7.7.1 through 7.7.3, except do not readjust the voltages). Set the READ 1/READ 7 Switch to READ 1.
- 8.2.5 Adjust the pulse generator frequency to 500 ± 1.0 KHz. Set the DATA PATTERN and ADDRESS PATTERN switches to SEQ. Push the START pushbutton. Measure and record, in the data sheet, the operating power (paragraphs 7.7.5 through 7.7.7, except adjust the voltages to $+5.25 \pm 0.02$ V and -6.40 ± 0.02 V).
- 8.2.6 Adjust the pulse generator frequency to 600 ± 1.0 KHz. Set the READ 1/READ 7 Switch to READ 7. Set the +5V supply to +4.75 ± .02V and the -6.1V supply to -5.80 ± .02V. Turn off the chamber and push the RESET pushbutton. The memory shall run without error for two minutes. Depress the STOP button. Record the results in the data sheet. Set the READ 1/READ 7 Switch to READ.1. Push the START button and readjust the voltages to 4.75 and -5.8. Push STOP.
- 8.2.7 Turn on the chamber and allow it to cool for 5 minutes.

 Then turn off the chamber and proceed to paragraph 8.2.8.
- 8.2.8 Repeat paragraph 7.13.1 through 7.13.4.
- 8.2.9 Set the MEMORY POWER switch to ON. Depress and release the START button. Using the DVM, adjust the memory power supplies to $+5.25 \pm 0.02$ V and -6.40 ± 0.02 V. Depress the STOP button.
- 8.2.10 Turn on the chamber and allow it to cool for 5 minutes.

 Then turn off the chamber and proceed to paragraph 8.2.11.

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- 8.2.11 Repeat paragraphs 7.13.1 through 7.13.4.
- 8.3 INTERMEDIATE TEMPERATURE TEST

 Set the chamber HEAT SELECTOR to the 375W position and the temperature to +85°C. Record the time.
- 8.3.1 Push the Reset and START buttons. Using the DVM, adjust the memory power supplies to $\pm 5.0 \pm 0.2$ V and -6.1V $\pm .02$ V. Depress the STOP button.
- 8.3.2 At 10 minute intervals record the thermistor resistance and repeat paragraphs 7.13.1 thru 7.13.4 except that each test will be run for 1 minute.
 - NOTE: When the thermistor indicates the internal temperature of the MEMORY is between 0°C and 15°C open the chamber and remove the plastic bag from the memory. Reseal the chamber.

Testing may be discontinued when the THERMISTOR indicates +75°C.

- 8.3.3 When the chamber temperature reaches $+85^{\circ} \pm 3^{\circ}$ C record the time on the data sheet.
- 8.4 HIGH TEMPERATURE

Beginning 50 minutes after the temperature chamber has reached 85°C measure and record the thermistor resistance at 10 minute intervals.

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8.4 (cont.)

At each measurement except the first one calculate the percentage change from the previous reading. When the change is less than 5 percent, proceed to paragraph 8.4.1.

- 8.4.1 Set the ADDRESS PATTERN and DATA PATTERN switches to SEQ.

 Turn the MEMORY POWER to ON. Using the DVM, adjust the memory power supplies to +5.25 ± 0.01V and -6.40 ± 0.02V.

 Measure and record the power supply voltage, current and standby (idle) power (paragraphs 7.7.1 through 7.7.3, except do not readjust the voltages). Set the READ 1/READ 7 Switch to READ 7.
- 8.4.2 Depress the START button. The memory shall run without error for 2 minutes. Record the results. Set the READ 1/READ 7
 Switch to READ 1.
- 8.4.3 Adjust the pulse generator frequency to 500 ± 1.0 KHz.

 Measure and record the operating power (paragraphs 7.7.5 through 7.7.7, except adjust the voltages to $+5.25 \pm 0.02V$ and $-6.40 \pm 0.02V$). Depress the STOP button. Adjust the pulse generator frequency to 600 ± 1.0 KHz.
- 8.4.4 Repeat paragraphs 7.13.1 through 7.13.4.
- 8.4.5 Set the MEMORY POWER switch to ON. Depress and release the START button. Using the DVM, adjust the memory power supplies to $+4.75 \pm 0.02$ V and -5.80 ± 0.02 V. Depress the STOP button.
- 8.4.6 Repeat paragraphs 7.13.1 through 7.13.4.

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8.4.7 Set the MEMORY POWER switch to ON.

Set the +5V supply to 5.0V ± .02 and the -6.1V and to -6.1 ± .02V. Set the DATA PATTERN switch to MAN and the ADDRESS PATTERN switch to SEQ. Set the READ/WRITE switch to WRITE. Select a random pattern and push the START pushbutton. The tester will write the data once in each of the 4096 addresses and stop. Set the READ/WRITE switch to READ and push the START pushbutton. The memory shall run without error. After 2 minutes, push the STOP button. Record the results. Set MEMORY POWER to OFF.

- 9. VACUUM TEST
- 9.1 SETUP
- 9.1.1 Verify that the MEMORY POWER switch on the Interface Box is in the OFF position. Turn the voltage controls fully counter-clockwise on all three power supplies.

Connect the equipment as shown in Figure 3.

Turn on power to all memory associated test equipment.

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9.1.2 Set the Tester and Interface Box controls as follows and maintain these control settings unless otherwise directed in the individual tests.

CONTROL	SETTING
ESTER	
BD1-BD4 (24 Switches)	UP
Tape Reader Power	Light Off
Run-OFF-Rewind Switch	OFF
Tester Power	Light ON
ADDRESS Switches	DOWN
DATA Switches	DOWN
READ/WRITE	READ
WORD LENGTH	24
READ 1/READ 7 Switch	READ 7
ADDRESS PATTERN	SEQ
DATA PATTERN	SEQ.
FREQUENCY	EXT
INTERFACE BOX	
MEMORY SELECT SWITCHES	A11 2.4V
INPUT CURRENT SWITCH	GND
OUTPUT PULLUP RESISTOR	≯5 V
INITIATE PULSE SWITCH	PULSE
WC2 SWITCH	OFF
WC SWITCH	OFF
MEMORY POWER	OFF

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- 9.1.3 Push the STOP button. Turn on all three power supplies. Using the DVM, adjust the Interface Box supply to $+5.0 \pm 0.1$ V. Set the memory supplies to approximately +5V and -6V. Set the MEMORY POWER switch to ON. Using the DVM, adjust the memory supplies to $+5.0 \pm 0.1$ V and -6.1 ± 0.1 V. Set the memory power switch to OFF.
- 9.1.4 Using the scope, adjust the Pulse Generator for $+3.0 \pm 0.1$ V positive pulses of 450 ± 10 nanoseconds duration (measured at the 50% points). Using the counter, adjust the rep rate to 600 ± 1.0 KHz. The pulse generator must be terminated in 50 ohms and connected to the tester when making these adjustments. Just prior to starting the environmental test, proceed to the next applicable paragraph.
- 9.2 TEST

Push the tester STOP and RESET pushbuttons. Turn the MEMORY POWER ON and push the START pushbutton on the tester. The tester will write a "0", read a "0" seven times in all data bits, write a "1", read a "1" seven times in all bits, step to the next address and repeat the same sequence. The tester will keep cycling until an error occurs. Record any bit errors. Proceed immediately to paragraph 9.2.1.

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- 9.2.1 While monitoring the tester for errors, start the vacuum chamber pump and pump the air out of the vacuum chamber at a rate such that the pressure inside the chamber drops to 7 mmHg in less than five minutes. Record any errors.
- Continue pumping the chamber until the pressure 10^{-5} mmHg. In order to reach this pressure, the test may last several hours. Therefore, one hour after the test has started, the memory and tester may be turned off by pushing the STOP pushbutton on the tester, turning the MEMORY POWER OFF and turning the TESTER POWER OFF. After the chamber has reached 10^{-5} mmHg, test the memory as outlined in paragraph 7.13. Record any errors. Push the memory STOP pushbutton, turn the MEMORY POWER OFF, turn the TESTER POWER OFF and return the memory to one atmosphere pressure.

10. <u>VIBRATION TEST</u>

The following vibration tests are to be performed in three mutually perpendicular axes. The tests include sine sweep and random vibration, and the levels to be used are described below in the individual tests. These levels are inputs to the base or mounting bracket of the unit under test. The unit shall be functionally tested during the vibration testing to insure correct operation. Prior to performing the random vibration a spectral analysis of the tester input shall be performed to insure that the random vibration input is within the specified limits. The analysis

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shall be plotted and the data sheet kept as part of the test data. For information only, an accelerometer shall be mounted on the top surface of the housing while testing the X and Z axes. Plot the output from this accelerometer and file as part of the test data.

- 10.1 SINE SWEEP TEST
- 10.1.1 Verify that the MEMORY POWER switch is in the OFF position.

 Turn the coarse voltage controls fully counterclockwise on all three power supplies.

Connect the equipment as shown in Figure 3 and turn on power to all memory associated test equipment.

Perform paragraphs 9.1.2, 9.1.3, and 9.1.4.

Mount the memory unit on the shake table so as to be vibrated in the vertical (Y) axis as shown in Figure 4. (The axis order may be varied for convenience).

10.1.2 Push the STOP and RESET buttons. Turn the MEMORY POWER ON.

Perform a sine sweep over the fequency range of 5-2000 Hz at
the levels listed below:

FREQUENCY RA	NGE	 TEST	LEVEL
5-25 Hz		0.33	in DA
24-110 Hz		10 G	PEAK
110-2000 Hz		5g	DEAK

The sweep rate is to be 2 octaves per minute. During the sweep, repeatedly perform the tests of paragraph 7.13. Record any bit errors in the Qual Test Data Sheet. Push the STOP button.

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- 1.0.2 RANDOM VIBRATION
- 10.2.1 Perform the spectral analysis specified in paragraph 10.

 While applying the following random vibration input, repeatedly perform the tests of paragraph 7.13.

FREQUENCY RANGE	TEST LEVEL	TOLERANCE		
15 Hz	$.0044\mathrm{g}^2/\mathrm{Hz}$	<u>+</u> 3db		
15-70 Hz	LINEAR INCREASE	Log-Log Plot		
70-100 Hz	.138 g ² /Hz	<u>+</u> 3db		
100-400 Hz	LINEAR DECREASE	Log-Log Plot		
400-2000 Hz	$.0089 \text{ g}^2/\text{Hz}$	± 3db		

The test time is to be 2 minutes per axis.

Record any errors in the Data Record.

- 10.22 Repeat paragraph 10.1.2 and 10.2, in the two other mutually perpendicular axes as shown in Figure 4. Push the STOP button.

 Turn the MEMORY POWER OFF and then turn the TESTER POWER OFF.
- 11. SHOCK TEST

Two shocks in each direction shall be applied along the three mutually perpendicular axes of the LP RASM (total of 6 shocks).

11.1 SETUP

Verify that the MEMORY POWER switch is in the OFF position. Turn the coarse voltage controls fully counterclockwise on all three power supplies. Connect the equipment as shown in Figure 3 and apply power to all memory associated test equipment. Set the controls as shown in para. 9.1.2 and perform para. 9.1.3 and 9.1.4. Mount the LP RASM on the shock table so as to apply

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1	SCOTTSDALE, ARIZONA 85252	SCALE	REVIS	ION	SHEE	T 29

the shock in the vertical (Y) axis as shown in Figure 5.

(The axes order may be varied for convenience).

- 11.2 TEST
- 11.2.1 Push the STOP and RESET buttons. Turn the MEMORY POWER ON and push the START button. The tester is now testing the LP RASM for bit errors. Apply a half sine shock pulse of 30 g's for a duration of 6 milliseconds. Record any bit errors. Push the STOP button.
- 11.2.2 Push the RESET and START buttons.

 Apply a half sine shock pulse of 30 g's for a duration of 12 milliseconds. Record any bit errors.
- 11.2.3 Repeat para. 11.2.1 and 11.2.2 for each of the other two directions as shown in Figure 5. Push the STOP button. Turn the MEMORY POWER OFF and then turn the TESTER POWER OFF.
- 12. FINAL FUNCTIONAL TESTS

To insure that the memory is still operating properly, perform all the tests of paragraph 7. Record the data.

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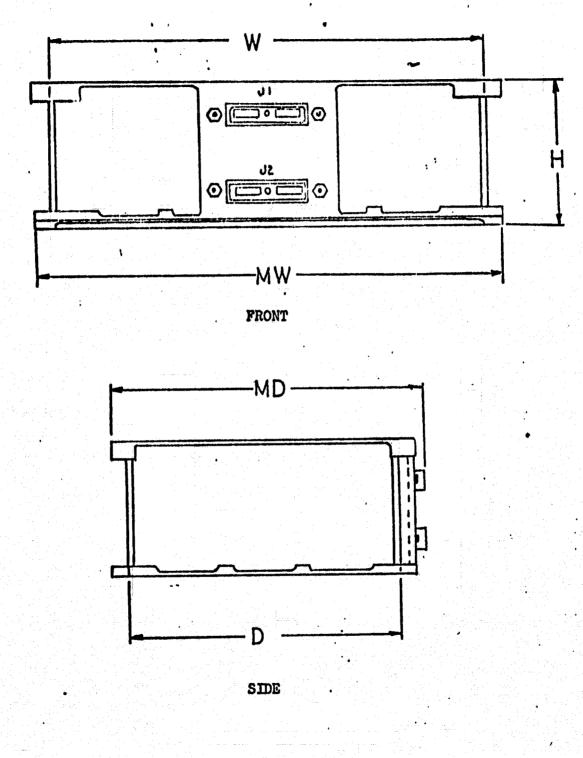


FIGURE 1. LP RASM OUTLINE DIMENSIONS

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MOTOTOLA ING.	SIZE	CODE IDE	ri no. j	DWG NO.				

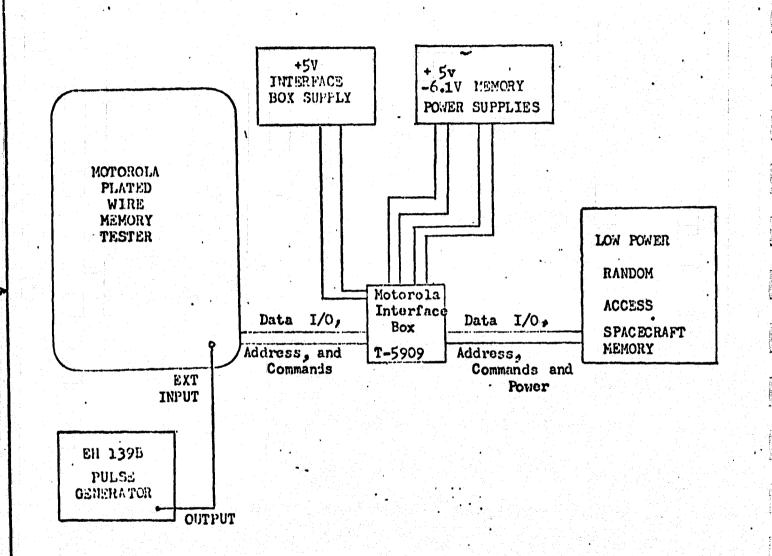


FIGURE 2. TEST SET UP

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	\$201 E. McDOWELL ROAD	<i>N</i>	34330	12-P13722D		
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	MOTOROLA INC.	SIZE	CODE IDENT NO.	DWG NO.	•	

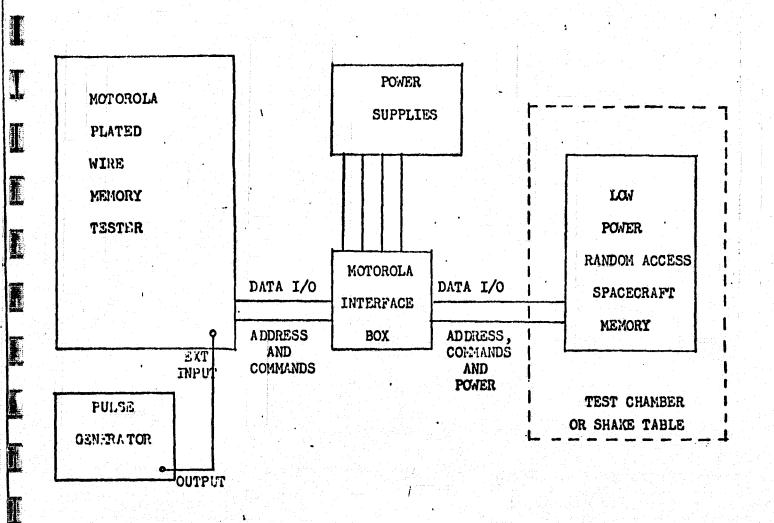
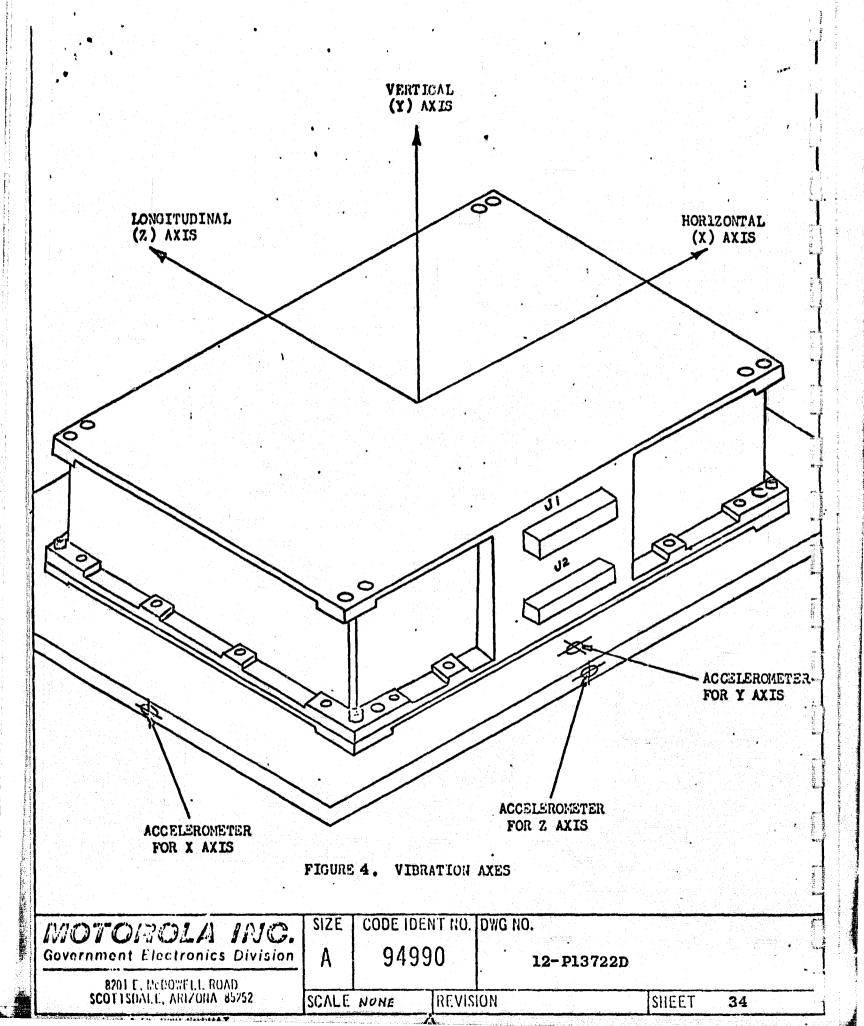
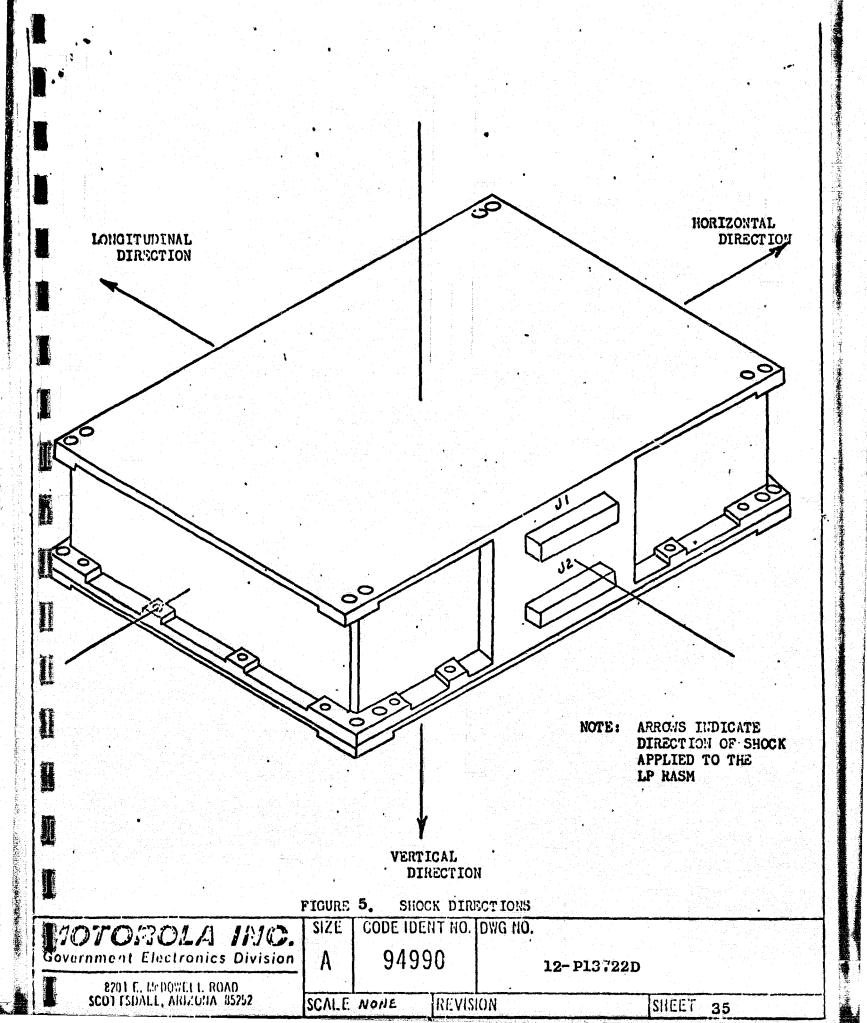


FIGURE 3. TEST SET UP

MOTORIOLA ING.	SIZE	CODE IDENT NO.	DWG NO.	
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ATTACHMENT II

ACCEPTANCE TEST DATA SHEET
LOW POWER RANDOM ACCESS
SPACECRAFT MEMORY
PART NO. 01-P13701D
SERIAL NUMBER 103
(35 PAGES)

#'APPLII	CATION	1	KENIZIUNZ		
EXT ASSEMBLY		LTR	DESCRIPTION	DATE	APPROVED
		Хl	Initial Release	,	
		X2	Incorporated changes prior, to First Usage	3-16-73	4. Luci
,	,,	Х3	Change -6.9V to -6.1V	6 18-73	1 Lever
ASTERISK INDICATES WHICH IS NONMANDA FOR INFORMATION	DATA ATORY	X4	Change 6000mw to 7000mw, pages 10, 17, 19, 30. Change weight from 6.0 to 6.5 pounds, page 2.	7-24-73	N. Jenes
		Х5	Add weight 5.8 pounds for magnesium chassis MCO S7835.	2-10-75.	Lame L
4601		, X6	Revised per MCO 57845	4-28-75	Semi.
م د د د د د د د د د د د د د د د د د د د					
* area					
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}EV	ΧI	X4	X1	хз	X1	X1	X1	X1	X1																				
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EV STATU	S	RE	٧	K 5	X 5	X1	X1	X1	X1	X1	X1	X1	х4	X1	X1	X1	X1	X1	Xe	XC	xe	Х6	X6	X1	X1	X1	X1	X1	X
OF SHEETS		SHE		1	2	_	4	5	6		8					_					_		7				24		
FOR ASSOCIA	TEC	LIS.	TS SE	E		<u> </u>			- بين		.				<u> </u>														-
INTERPRET					RDAN	CE V	HTIV	STAP	IDAR	DS P	RES	CRIB	ED E	Y															-

NLESS OTHERWISE SPECIFIED OR BY H. Tweed 8201 EAST McDOWELL ROAD ALL DIMENSIONS ARE IN INCHES AND END USE. FOR TOLERANCES SEE NOTE MOTOROLA INC. SCOTTSDALE, ARIZONA 85252 CHK BY Government Electronics Division CONTR NASS-23163
NO. NASS-20576
RELEASE
NOTICE
APPROVE 4339 4601 AATERIAL: ACCEPTANCE TEST DATA SHEET, LOW POWER RANDOM ACCESS SPACE-CRAFT MEMORY, PART NO. 01-P13701D CODE IDENT NO. DWG. NO. APPROVED DATE SIZE 1-2-73 94990 12-P13721D **APPROVED** SCALE SHEET 1 OF 35

Y-1-C-19911-10UA-7/70 DWG FORMAT

1. SCOPE

This test data sheet is to be used to record data as required by the Acceptance Test Procedure for the Low Power Random Access Spacecraft Memory.

- 2. REFERENCE INFORMATION
- 2.1 SPECIFICATIONS APPLICABLE

S-562-P-24

Low Power Random Access Spacecraft Memory

12-P13722D

Acceptance Test Procedure, Low Power Random Access Spacecraft Memory

3. TEST DATA

Unit S/N /03 Start Dat

Start Date of Tests

4/28/75

Tested by _____

ATP PARA. NO.

EQUIVALENT TEST EQUIPMENT 3.1 428A DC MILLIAMMETER HIP 585A OSCILLUSCOPE TEK FLUKE BIZUA DILIMAL VOLTMEITER 57.45L GOUN FER HIP POWER SURFY 6050 A POWER DIYEN

4. PHYSICAL CHARACTERISTICS

Limit

6.1 WEIGHT

Weight of LP-RASM - 5,640 Pounds

6.5 pounds (aluminum)

5.8 pounds (magnesium)

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8/N <u>/03</u>

Date of Test 4/28/25.
Tested By B-Ka-tf

6.2 DIMENSIONS

Limit

H = 2.896 inches

M = 8.960 inches

W- 8,630 inches

D = 6.322 inches

MD- 6.929 inches

V - H X W X D - 158.0 inches³

≤ 160 inches³

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7.4	CHASSIS ISOLATION	Limit
•	Impedance 7 11.999 MF 60HM3	≥ 9 megohms
7,5	INPUT SIGNAL LOADING	
7.5.2	Current from INITIATE PULSE to Gnd 1.15 ma	≤ 2 ma
	Current from 2.4V to INITIATE PULSE 3.43 µa	≤ 20 µa
7.5.3	Current from MEM SEL 1 to Gnd 1/14 ma	≥ °2 ma.
	Current from 2.4V to MZM SEL 1 2.49 µa	≤ 20 y a
7.5.4	Current from MEM SEL 2 to Gnd /1/4 ma	≤ 2 ma
•	Current from 2.4V to MEM SEL 2 3,46 ya	≤ 20 µa
	Current from MEM SEL 3 to Gnd ///4 ma	≤ 2 ma
	Current from 2.4V to MEL SEL 3 3.42 ya	≤ 20 µ a
	Current from MEM SEL 4 to Gnd 1-14 ma	≤ 2 ma
•	Current from 2.4V to MEM SEL 4 2.49 ya	±20 µa
7.5.5	Current from READ/WRITE to Gnd856 ma N	≤ 2 ma
	Current from 2.4V to READ/WRITE -356 49 4	≤ 20 µa
7.5.6	Current from ADDRESS 20 to Gnd87ma	≤ 2 ma
	Current from 2.4V to ADDRESS 20 5.28 pa	≤20 µa
	보면하는 그는 사람들이 수가로 가는데 하시겠다. 그는 물을 먹어 보다	

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	Limits
Current from ADDRESS 2 to Gnd	≰ 2 ma
Current from 2.4V to ADDRESS 21 5.06 pa	€ 20 Ha
Current from ADDRESS 22 to Gnd _945 ma	≤ 2 ma
Current from 2.4V to ADDRESS 22 5.68 pa	≤ 20 µ a
Current from ADDRESS 23 to Gnd _882 ma	≤ 2 ma
Current from 2.4V to ADDRESS 23 5.36 µa	≤ 20 ₁ , a
Current from ADDRESS 24 to Gnd .934 ma	≤ 2 ma
Current from 2.4V to ADDRESS 24 6./a	± 20 µa

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8/N <u>103</u>			of Test 4/28/75.
	ADD&2SS 2 ⁵ to Gnd 2.4V to ADDRESS 2 ⁵		Limits 2 ma 20 20 20
Current from	ADDRESS 2 ⁶ to Gnd 2.4V to ADDRESS 2 ⁵	.870 ma	∠ 2 ma ∠ 20 µ a
	ADDRESS 2 to Gnd		≤ 2 ma ≤ 20 Na
	ADDRESS 28 to Gnd		∠ 2 ma ∠ 20 Na
	n ADDRESS 29 to Gnd		∠ 2 ma ∠ 20 μa
Current from	n ADDRESS 2 ¹⁰ to Gnd n 2.4V to ADDRESS 2 ¹	.852 ma .0 5,46 µa	ے 2 ma 4 عر 20 کے
	n ADDRESS 2 ¹¹ to Gnd		≤ 2 ma ⊆ 20 μa
	n DATA IN BIT 0 to G		∠ 20 ma ∠ 20 μa

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CODE IDENT NO. DWG NO.

	8/N	103					st 4/28/2 B. For	75
		•				,		
	4						Limits	
	Current	from	DATA	IN	BIT 1 to Gnd 104 ma		≤ 2 ma	1 .
	Current	from	2.4V	to	DATA IN BIT 1 8/2 pa	. ***	∠ 20 Na	
	Current	from	DATA	IN,	BIT 2 to Gnd 1.06 ma		≤ 2 ma	
				•	DATA IN BIT 2 7,45 Na		€ 20µa	
	Current	from	DATA	IN	BIT 3 to Gnd 1996 ma	•	_ _ 2 ma	
					DATA IN BIT 3 8,7 pa		≤ 20/2a	
	Current	from	DATA	IN	BIT 4 to Gnd 1,00 ma		<u>∠</u> 2 ma	
					DATA IN BIT 4 8.62 Ma		∠ 20/Ua	
•	Current	from	DATA	IN	BIT 5 to Gnd 1,024 ma		∠ 2 ma	* * * * * * * * * * * * * * * * * * *
					DATA IN BIT 5 8,72 pa	·	€20µa	
	Current	from	PATA	IN	BIT 6 to Gnd 1.05 ma	•	<u>∠</u> 2 ma	
	ng district the				DATA IN BIT 6 7,0 pa	• • • •	≤20 Ma	
	Current	from	DATA	IN	BIT 7 to Gnd ma		<u>2</u> 2 ma	
	Current	from	2.4V	to	DATA IN BIT 7 7,53 pa		≤ 20 Na	
	Current	from	DATA	IN	BIT 8 to Gnd /1.04 ma		<u></u> ∠ 2 ma	
					DATA IN BIT 8 7.54 pa		₹20µa	
	Current	from	DATA	IN	BIT 9 to Gnd		≤ 2 ma	
					DATA IN BIT 9 3.06 µa		< 20 Ma	

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					Limits
Current	from	DATA	IŅ	BIT 10 to Gnd	. <u>£</u> 2 ma
Current	from	2.4V	to	DATA IN BIT 10 3.// pa	£ 20/2a
Current	from	DATA	IN	BIT 11 to Gnd <u>.972</u> ma	<u>∠</u> 2 ma
Current	from	2.4V	to	DATA IN BIT 11 2,92 Na	£ 20/08
Current	from	DATA	IN	BIT 12 to Gnd 306 ma	<u>∠</u> 2 ma
Current	from	2.4V	to	DATA IN BIT 12 7,23 pa	≥20µa
Current	from	DATA	IN	BIT 13 to Gnd ma	≤ 2 ma
Current	from	2,40	to	DATA IN BIT 14 7.47 pa	∠ 20 μa
Current	from	DATA	IN	BIT 14 to Gnd	∠ 2 ma
Current	from	2.4V	to	DATA IN BIT 14 S,02 pa	≥ 20µa
Current	from	DATA	IN	BIT 15 to Gnd <u>1950</u> ma	∠ 2 ma
Current	from	2.4V	to	DATA IN BIT 15 4,97 pa	€ 20 µa
Current	from	DATA	IN	BIT 16 to Gnd ma	≤ 2 ma
				DATA IN BIT 17 5,03 µa	€ 20 µa
Current	from	DATA	IN	BIT 17 to Gnd <u>.929</u> ma	∠ 2 ma
Current	from	2.4V	to	DATA IN BIT 17 5.13 Na	≥ 20 pa

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7,6,3

7,6,4

DATA OUT BIT 2 voltage DATA OUT BIT 3 voltage - // DATA OUT BIT 4 voltage - /0 ≤ 100 mv DATA OUT BIT 5 voltage -/O mv ≤ 100 mv DATA OUT BIT 6 voltage -/0 mv **= 100 mv** DATA OUT BIT 7 voltage mv **≤ 100 mv** DATA OUT BIT 8 voltage mv **≤** 100 mv DATA OUT BIT 9 voltage mv ≤ 100 mv DATA OUT BIT 10 voltage mv ≤ 100 mv -/0 DATA OUT BIT 11 voltage mv ≤ 100 mv= DATA OUT BIT 12 voltage mv ≤ 100 mv DATA OUT BIT 13 voltage mv € 100 mv 20 DATA OUT BIT 14 voltage mv ≤100 mv -10 DATA OUT BIT 15 voltage ≤100 mv DATA OUT BIT 16 voltage - 20 ≤ 100 mv

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DATA OUT BIT 17 voltage

•	s/n <u>103</u>	Date of Test 4/28/75 Tested By B 60
		Limits
7.7	POWER CONSUMPTION (25°C)	
7.7.1	Memory +5V Voltage 4,993 Volts	
	Memory -6.1V voltage - 6.102 Volts	
	+5V Current	4.1
	+5V Power 57,5 mw	4.7
7.7.2	Memory -6.1V Current 4.7 ma	244
	Memory -6.1V Power <u>28.7</u> mw	
7.7.3	Total Memory Idle Power 35.4 mw 80.2	170 mw max
7.7.5	Memory +5V Voltage 5,006 Volts	
	Memory -6.1V Voltage 6./6/ Volts	
	+5V Current 695 ma	695
	+5V Power 3475 mw*	31175 6.47
7,7,6	Memory -6.1V Current 240 ma	3,90
	Memory -6.1V Power /4/04 mw	3.4.75 240 14 40 14 64.0
	4 9 3 9	
7,7,7	Total Active Power 7767 mw	7000 mw max.
7.8	READ COMPLETE TIMING	
7.8.5	Delay $\frac{4/0}{}$ ns	500 ns max.
	Duration 330 ns	250 ns min 450 ns max.
		200 IIS WAX.
		@ MAS.
MOTO	DROLA INC. SIZE CODE IDENT NO. DWG NO.	tore.
	at Electronics Division A 94990	12- P13721D

AV.2.0.1000 1004.2.40 DWG FORMAT

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5 / 1	N <u>105</u>		Date of Test	B. for
8.7 &	READ CO	MPLETE/DATA OUTPUT TI	MING	LIMITS
8.8	DO- 0	OK REJECT		
	DO-1	OKREJECT_	· · · · · · · · · · · · · · · · · · ·	
	DO-2	OKREJECT_		
	DO-3	OKREJECT	•	
	DO-4	OK REJECT	· · · · · · · · · · · · · · · · · · ·	
	DO-5	OKREJECT_		
	DO-6	OKREJECT		
•	DO-7	OK REJECT		REFER TO
	DO-8	OKREJECT		TEST PROC.
	DO-9	OKREJECT		
	DO-10	OKREJECT		
	DO-11	OKREJECT		
	DO-12	OKREJECT		
	DO-13	OKREJECT_		
	DO-14	OKREJECT		
	DO-15	OKREJECT		
	DO-16	OKREJECT		
	DO-17	OKREJECT_		

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	s/n 103		Date of Test Tested By	4/20/7
				Limits
7.9	SYSTEM FUNCTIONAL TE	ST		
7,9,2	Did an error occur?			
	Yes Address	Bits		0 errors
7.9.4	Did an error occur?			
	Yes Address	Bits		0 errors
7.9.10	Did an error occur?			
	Yes Address	Bits		0 errors
7.9.16	Did an error occur?			
	Yes Address	Bits		0 errors
7.10	RANDOM ACCESS CAPABI	ILITY		
7.10.6	Did an error occur?			
	Yes Address	Bits		0 errors
7.10.7	Did an error occur?			
	Yos Address	Bits		0 errors
				@ Whs.
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	t Electronics Division	94990	12-P137	21D

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SCALE

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The state of the s	s/n <u>103</u>	Date of Test	4/28/75
		Tested By	Limits
	b) No		
*	Yes Address	Bits	0 errors
	c) No Address	Bits	0 errors
7.11	NON-VOLATILITY TEST		
7.11.7	Did an error occur?		
& Statute CT 13 0	No /		
7.11.9	Yes Address Bits		0 errors
7.12	MEMORY SELECT TEST		
7.12.3	Address <u>ecoo</u> (Octal)		0000
7.12.4	Address 0001 0000 (Octal)		0000
	0010 <u>0000</u> (Octal)		0000
	0011 (OCC) (Octal)		0000
	0100 (Octal)		0000
	0101 <u>COCO</u> (Octal)		0000
	0110 <u>0000</u> (Octal)		0000
	0111 <u>0000</u> (Octal)		0000
	1000 <u>ONON</u> (Octal)		0000
	1001 (Octal)		0000
	1010 <u>0000</u> (Octal)		0000
			MS

65FC

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G	ov	orn	me	nt	EI	ect	ron	ics	Di	vis	ioi	n
-												-

A

SIZE

12-P13721D

8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

REVISION SCALE

CODE IDENT NO. DWG NO.

94990

, , , , , , , , , , , , , , , , , , ,	s/n <u>103</u>	Date of Test Tested By	6,60
			Limits
•	Address 1011 <u>COCO</u> (Octal)		0000
	1100 (0000 (Octal)		0000
· - · · · · · · · · · · · · · · · · · ·	1101 @@@@ (Octal)		0000
	1110 @@@@ (Octal)		0000
.12.6	Did an error occur?		
	No		
•	Yes Address Bits		0 errors
.13	WORST CASE PATTERN TEST		
.13.2	Did an error occur?		
7.	No		
	Yes Address Bits		0 errors
.13.3	Did an error occur?		
	No		
	Yes Address Bits		0 errors

@ //	1/	1	D
	5/-	7	

MOTO	ROLA:	INC.
Government	Electronics	Division
-		

8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252 A 94990

SIZE

SCALE

CODE IDENT NO. DWG NO.

12-P13721D

REVISION SHEET , 14

•	s/n <u>105</u>			Date of Test 4/28/79 Tested By B. Joy
7.13.4	The state of the s	error occur?		Limits
	No	Address	Bit	. 0 errors
	b) Did an	error occur?		
	Yes	Address	Bit	0 errors
				@ MAS 65FC
	COLA IN	SIZE COD	E IDENT NO. DWG NO.	

S/N /6		•	•			DATE O	F TEST	4/2-	1/75
					• .		BY		W
				•			·		
8.	TEMPERATURE TE	ST			•	•		LIMI	rs
8.2.1	TIME 5:57						•		· ·
8.2.2	LOW TEMPERATUR	E			•				
	THERMISTOR RES	ISTAN	CE						**************************************
	150 MINUTES 2	22. <u>3</u>	K OHM	5				•	
	160 MINUTES 22	2,7	_ K OHM	S % C	HANGE	12%:	•		
	170 MINUTES		к онм	s % (HANGE	, ,	•		
	180 MINUTES		_ к ония	s % c	HANGE			•	
	190 MINUTES		к онм	5 % C	HANGE		•		e e
					•			•	1
8,2,3	DID AN ERROR O	CCUR?	•		•				
	NO V		•		•		•		***
	YESA	DRESS	3	_	BITS_			O ER	RORS
994	A 1 V VOI TACE	/ .l.a.	/ 	; - :	. E W	VOLTACE	واريد س	VOT MO	
9,6,3	-6.1 V VOLTAGE								
	-6.1 V CURRENT	14.3		•		CURRENT			
	-6.1 V POWER	91,5	2 mw		+5 V	POWER	57.26	DW ;	
	TOTAL MEMORY II	OLE PO	OWER 148.7	8 mw				170 mw	MAX
8.2.5	-6.1 V VOLTAGE	6.40	2 VOLTS		+5 V	VOLTAGE	5.25	VOLTS	
	-6.1 V CURRENT	26	∑ ma		+5 Y	CURRENT	700	ma	
	-6.1 V POWER	1.68] mw	•	+5 Y	POWER	3,675,		
							•		
	TOTAL MEMORY OF						.12/	7000 m	H MAX
	POLA INC.	SIZE	CODE IDEN		DWG NO				· • • • • • • • • • • • • • • • • • • •
	lectronics Division	A	9499	0	1,, 1	12	2-P1372	1D	-
SCOTTSDA	McDOWELL ROAD LE, ARIZONA 85257	SCALE		REVIS	ION		SHE	ET 16	

5/N . /	0.3	•	DATE (OF TEST 4/2-9/75
		•	TESTEI	BY B fox
		•		
		•		LINITS
8.2.6	DID AN ER	ROR OCCUR?		
	NO V	•	•	
	YES	ADDRESS	BIT	O ERRORS
• • • • • • • • • • • • • • • • • • • •	•			
8.2.8		D AN ERROR OCCUR?		
*	NO _			
	YES	ADDRESS	BIT	O ERRORS
	WC b) DID	AN ERROR OCCUR?		
	NO V	am amon occur		
	* * * * * * * * * * * * * * * * * * * *	ADDRESS	віт	A EPPAPE
	YES	ADDRESS	— BII ———	_ O ERRORS
	WC c) DID	AN ERROR OCCUR?		
	NO V			
	YES	ADDRESS	BIT	O ERRORS
	MC q) DID	AN ERROR OCCUR?		
	NO V			
	YES	ADDRESS	BIT	_ O ERRORS
8.2,611	WC a) DID	AN ERROR OCCUR?		
	NO V			
	YES	ADDRESS	BIT	O ERRORS
				will a
	·			ESFC 3
MOTOF	POLA II	NC. SIZE CODE IDE		
overnment E	lectronics Di	ivision A 9499	0	, ^ 12 -P13721D
	「McDOWELL ROA Ale, arizona 85		REVISION	CHEET 17

•			,				
5/N	103			•	DATE OF TES	r <u>4/</u>	124/75
	21.111			•	TESTED BY	B.	
	•	•	•		· · · · · · · · · · · · · · · · · · ·	LI	MITS
8.2.9	(Cont.)	•		•	•		•
	MC P) DI	ID AN ERROR	OCCUR?		e de la companya de La companya de la co		
	NO V			•	•		
	YES	ADDRE	ss	BIT		.0	ERRORS
	WC c) DI	ID AN ERROR	OCCUR?	•		· · · · · · · · · · · · · · · · · · ·	
	NO /					•	
	YES	ADDRE	ss	BIT		. 0	ERRORS
	WC d) Di	ID AN ERROR	OCCUR?	•			
	NO /			•			•
•		ADDRE	ss	ВІТ	-	•	ERRORS
8.3		DIATE TEMPER	ATURE TEST				
	TIME)	<u> </u>	1	•	,		
8.3.2	TIME	THERMISTOR	READING.	DID ANY	ERROR OCCUR?	i i i i i i i i i i i i i i i i i i i	
	9.15	176.8	K OHMS	NO V	YES		ERRORS ERRORS
	10.05	57,00	K OHMS	NO NO	YES YES	0	ERRORS ERRORS
	10.35	9.38	K OHMS	NO W	YES	0	ERRORS ERRORS
	10:45	5-77	K OHMS	NO W	YES YES	0	ERRORS ERRORS
	11:05	2.73	K OHMS	NO V	YES THE	0	ERRORS ERRORS
			K OHMS	NO	YES	. 0	ERRORS ERRORS
					n	175-	
MOTO	ROLA	INC SIZE	CODE IDEN	T NO. DWG NO		19.57C	
	Electronics		94990	0	12-P13	3721D	
			1	ſ		•	

8201 EAST MCDOWELL ROAD SCOTTSDALE, ARIZONA 85257

SCALE REVISION

8/N/	03		DATE	OF TEST	129/75
	·	•	TEST	ED BY	- FAT
	•				
		•			LIMITS'
8.3.3	TIME 10:54		•		
8.4/60	50 MINUTES 1.4	HOB K OHMS			
	80 MINUTES		% CHANGE		
et	TO MINUTES		•		
	80 MINUTES				
	90 MINUTES			,	
					7 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 -
8.4.1	-6.1 V VOLTAGE	6.40 SVOLTS	+5 V VOLTAGE	5,252 yolts	
	-6.1 V CURRENT	6.3. ma	+5 V CURRENT	12.2 ma	
	-6.1 V POWER	40.3 mw	+5 V POWER	61.1 mw	
4. <u>*</u>	TOTAL MEMORY II	LE POWER	<u>1.4</u> mw	17	O mw MAX
8.4.2	DID AN ERROR OC NO YES	CCUR?	BIT		O ERRORS
and All Control of the Control of th	•		•	· · · · · · · · · · · · · · · · · · ·	
8.4.3	-6.1 V VOLTAGE	6.400 VOLTS	+5 V VOLTAGE	5.247 VOLTS	
	-6.1 V CURRENT	280 ma	+5 V VOLTAGE	795 ma	
	-6.1 V POWER	1772 mw	+5 V POWER	4171 mw	
STATE OF THE STATE	TOTAL MEMORY OF	PERATING POWER	5963 m	v - 70	00 mw MAX
8.4.4	WC a) DID AN EI	RROR OCCUR?			
	NO V				
	YES	IDDRESS	BIT	<u> </u>	O'ERRORS
	A	LAUTE LAGGE			SPC
	ROLA INC. lectronics Division	SIZE CODE IDEN		12-P1372 1D	
	MCDOWELL ROAD ALE, ARIZONA 85257	SCALE	REVISION	SHEET	19

s/n <u>103</u>	•		. DAT	e of test	1/29/2	<u>, -</u> [
	•	•	TES	TED BY	- First	_]
8.4.4 (Cont.)	•				LIMITS	~
WC b) DID AN EI	RROR O	CCUR?			•	**
NO V		•				44 916
YES	ADDRES	S	BIT	• • • • • • • • • • • • • • • • • • •	O ERRORS	***
WC c) DID AN E	RROR O	CCUR?				
NO V		• *************************************				- 18 18 73
YES to the	ADDRES	S	BIT		O ERRORS	: *** !
WC d) DID AN E	RROR O	CCUR ?				*
NO _		1	**************************************			7
YES	ADDRES	s	BIT		O ERRORS	1
8.4.6 WC a) DID AN E	RROR O	CCUR?				1000 1000 1000 1000 1000 1000 1000 100
NO VES	ADDRES	S	BIT		O ERRORS	#*** 24
WC b) DID AN E	·• "·	3				¥
NO						
	ADDRES	·	BIT		O ERRORS	
WC c) DID AN E	KKUR C	ACUR?				
	ADDRES	is	BIT		O ERRORS	· Salar
WC d) DID AN E	RROR C	OCCUR?				
NO <u> </u>	ADDRES	IS 1000 100 100 100 100 100 100 100 100 1	BIT		O ERRORS	pressure
						(Tree)
8.4.7 DID AN ERROR O	CCUR?					ļ.
NO <u>\(\(\) \(\</u>						
YES	ADDRES	SS	BIT		O ERRORS	and the second second
To action to the second		0005 105 15	lowa ec		ESFE	
MOTOROLA INC. Divernment Electronics Division		code ident no. 94990	DWG NO.	12- P13721D		No. or other death
8201 EAST MCDOWELL ROAD SCOTTSDALE, ARIZONA 85257	SCALE	REVIS	I	SHEET	20	— [

AV-2-8-199H-100A-2 74 DWG FORMAT

• · · · · · · · · · · · · · · · · · · ·	S/N 103	Date of Test <u>5/5/75</u>
and the state of t		Tested by Bart
	6	Limits
9.	VACUUM TEST	
9.2	Did Any Bit Errors Occur?	
erenda erend Erenda erenda erend	No	
	YesAddressBit	ts 0 Errors
0.2.1	Fast Decompression	
	Date <u>5/5/75</u> Tested	by B port
	Did Any Bit Errors Occur?	
	No. 2 V	
	Yes Address B	lts0 Errors
9.2.2	Hard Vacuum 🛞	
	Date 5/5/75 Tested	d by B. LmT
•		Siz)
	Did Any Bit Errors Occur?	C veri
	No	
	YesAddress	- Bits 0 Errors
10.	VIERATION TEST	· ECM
	Date 5/6/75 Tester	d by 1xth.
	SINE SWEEP	
	Axis X - Did Any Bit Errors	Occur?
	No	
	YesFreqAddres	ssBits0 Errors

THE THE PROPERTY OF THE PROPER

MOTOROLA INC.	SIZE	CODE IDENT NO.	DWG NO.		
Government Electronics Division		94990		12-P13721	
8201 E. McDOWELL ROAD		<u> </u>			
SCOTTSDALE, ARIZONA 85252	SCALE	REVIS	ION		SHEET 21

•	S/N Date o	by the file
	Tested	by Chartel
	Axis Y - Did Any Bit Error Occur?	Limits
•	No	
	Yes Freq Address Bits	0 Errors
	Axis Z - Did Any Bit Errors Occur?	
	No V	(B) Jul
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Yes Freq Address Bits	
	RANDOM VIBRATION .	
	Axis X - Did Any Bit Errors Occur?	
	No V	
	Yes Freq Address Bits	
	Axis Y - Did Any Bit Errors Occur?	
	No <u>i</u>	
	Yes Freq Address Bits	0 Errors
	Axis Z - Did Any Bit Errors Occur?	
	No	Dun cond Test
	Yes Freq Address Bits	Jul No Not
		RERAU FOR PLOT
11.	SHOCK TEST	
	Date <u>5/8/75</u> Tested By	
	6 MILLISECOND DURATION SHOCK	
	Y Direction - Did Any Bit Errors Occur?	
	CVERTICAL) No	
	Yes Address Bits	0 Errors
The second secon	OFOLA INC. SIZE CODE IDENT NO. DWG NO	
-	ent Electronics Division A 94990	12-P13721D
	201 E. McDOWELL ROAD TTSDALE, ARIZONA 85252 SCALE REVISION	SHEET 22

Limits

No			
Yes	Address	Bits	0 Errors
X Direc	tion - Did Any Bit	Errors Occur?	
No			
	Address	Bits	0 Errors
12 MILL	ISECOND DURATION S	HOCK	
Y Direc	tion - Did Any Bit	Errors Occur?	
No L-			
Yes	Address	Bits	0 Errors
Z Direc	tion - Did Any Bit	Errors Occur?	
No			
Yes	Address	Bits	0 Errors
X Direc	tion - Did Any Bit	Errors Occur?	
No			
Yes	Address	Bits	0 Errors

		5-9-75.
en g	And the second s	
7,4	CHASSIS ISOLATION	<u>Limit</u>
arr.	Impedance >10	≥ 9 megohms
7.5	INPUT SIGNAL LOADING	
7.5.2	Current from INITIATE PULSE to Gnd ///64 ma	≤ 2 ma
	Current from 2.4V to INITIATE PULSE 3.57 pa	≤ 20 µa
7.5.3	Current from MEM SEL 1 to Gnd ///67 ma	< 2 ma
	Current from 2.4V to MEM SEL 1 2.52	≥ 20 µa
7.5.4	Current from MEM SEL 2 to Gnd 1166 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 2 3.59 ya	≤20 µa
	Current from MEM SEL 3 to Gnd	≤ 2 ma
	Current from 2.4V to MEL SEL 3 3.54 ya	≤ 20 µ a
	Current from MEM SEL 4 to Gnd /1/63 ma	≤ 2 ma
TANK.	Current from 2.4V to MEM SEL 4 2.56 pa	≤20 µ a
7.5.5	Current from READ/WRITE to Gnd 6.827 ma	≤ 2 ma
	Current from 2.4V to READ/WRITE 5.13 pa	≥20µa
7.5.6	Current from ADDRESS 20 to Gnd ma	≤ 2 ma
	Current from 2.4V to ADDRESS 20 5.47 pa	≤20 µa
	도하는 사용 마음이 생각을 위한 사용이 되는 것이 되는 것을 보고 있을 것이 하는 것이 하는 것이 되었다. 2000년 2월 1일	
	그로 보는 그는 그 전 등 전에는 그를 받았다. 하는 그는 그들은 독특분도 바로 모르게 되었다. 그는 마을 하는 것을 하는 것이 말했다. 그는 그는 그를 가는 것을 하는 것이 되었다.	N.w. Hefermer

8701 E. MCDOWELL ROAD SCOTTSDALL, ARIZONA 65/52

Government Electronics Division

A 94990

SCALE

REVISION .

12-P13721D

	Limits
Current from ADDRESS 2 to Gnd . 876 ma	≤ 2 ma
Current from 2.4V to ADDRESS 21 5.22 pa	≤ 20 µa
Current from ADDRESS 22 to Gnd	€ 2 ma
Current from 2.4V to ADDRESS 22 5.87 pa	≤ 20 µ a
Current from ADDRESS 23 to Gnd904 ma	. ≤ -2 ma
Current from 2.4V to ADDRESS 23 5.57 ma	≤ 20 _µ a
Current from ADDRESS 24 to Gnd .958 ma	≤ 2 ma
Current from 2.4V to ADDRESS 24 6.33 pa	. همر 20 ي

N.w. Hefferen 5-9-75



WOTOROLA INC.
Government Electronics Division

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SIZE

94990

CODE IDENT NO. DWG NO.

12-P13721D

8001 E. McDOWELL ROAD SCOTTSDALL, ARIZONA 85252

SCALE REVISION

103 Date of Test (-0-7 Tosted By Limits Current from ADDRESS 25 to Gnd . 905 ma **≤** 2 ma Current from 2.4V to ADDRESS 25 € 20 Na Current from ADDRESS 26 to Gnd . 84/ ma < 2 ma Current from 2.4V to ADDRESS 25 5.19 ع 20 ي Current from ADDRESS 27 to Gnd . 986 ≤ 2 ma Current from 2.4V to ADDRESS 2 5.85 Na ∠ 20/Va Current from ADDRESS 28 to Gnd ∠ 2 ma Current from 2.4V to ADDRESS 28 /.02 pa € 20 Na Current from ADDRESS 29 to Gnd ∠ 2 ma Current from 2.4V to ADDRESS 29 /.// /a £ 20 Na Current from ADDRESS 2 to Gnd ∠ 2 ma Current from 2.4V to ADDRESS 210 5.60 pa 4 20 Na Current from ADDRESS 211 to Gnd , 876 ma ≤ 2 ma Current from 2.4V to ADDRESS 211 5.57 Wa € 20 µa Current from DATA IN BIT 0 to Gnd /c 8 ma <u>∠</u> 2 ma Current from 2.4V to DATA IN BIT 0 9.21 pa 20 کے 7.4.w. 76ffered 5-9-15 SIZE | CODE IDENT NO. DWG NO.

8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

SCALE.

94990

12-P13721D

REVISION

		Limits
Current from DATA IN BIT 1 to	Gnd/. o6 ma	≤ 2 ma
Current from 2.4V to DATA IN B	and the second s	∠20 Na
Current from DATA IN BIT 2 to	Gnd /. 08 ma	∠ 2 ma
Current from 2.4V to DATA IN B		€ 20µ a
Current from DATA IN BIT 3 to	Gnd /,07 ma.	≼ 2 ma
Current from 2.4V to DATA IN E	_	≤ 20/Pa
Current from DATA IN BIT 4 to	Gnd 1.02 ma	≤ 2 ma
Current from 2.4V to DATA IN E		₹ 20/Ua.
Current from DATA IN BIT 5 to	Gnd /105 ma	<u>∠</u> 2 ma
Current from 2.4V to DATA IN I		≥ 20µa
Current from DATA IN BIT 6 to	Gnd /, 08 ma	<u>≤</u> 2 ma
Current from 2.4V to DATA IN I	BIT 6 _ 7.18 \ \mu a	<u>∠</u> 20,⁄~a
Current from DATA IN BIT 7 to	Gnd //c7 ma	∠ 2 ma
Current from 2.4V to DATA IN	BIT 7 7.80 pa	≤ 20/2a
Current from DATA IN BIT 8 to	Gnd <u>/.o.l.</u> ma	<u>∠</u> 2 ma
Current from 2.4V to DATA IN	BIT 8 7.77 pia	<u>≤</u> 20 ju a
Current from DATA IN BIT 9 to	Gnd .988 ma	<u>≤</u> 2 ma
Current from 2.4V to DATA IN	BIT 9 3.16 pa	Lefferin
	ライル・	Helforon

MOTOFIOLA INC.
Government Electronics Division

8201 C. MCDOWELL ROAD

SIZE CODE

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CODE IDENT NO. DWG NO. 94990

12-P13721D

DEMINISTR

	Limits
Current from DATA IN BIT 10 to Gnd .991 ma Current from 2.4V to DATA IN BIT 10 3.21 pa	∠ 2 ma ∠ 20µa
Current from DATA IN BIT 11 to Gnd .995 ma Current from 2.4V to DATA IN BIT 11 2.99 Pa	<u>د</u> 2 ma <u>د</u> 20 μ a
Current from DATA IN BIT 12 to Gnd	<u>∠</u> 2 ma <u>∠</u> 20µa
Current from DATA IN BIT 13 to Gnd835 ma Current from 2.4V to DATA IN BIT 14 7.67 \(\mu \) a	≤ 2 ma ≤ 20µa
Current from DATA IN BIT 14 to Gnd860 ma Current from 2.4V to DATA IN BIT 14 8 2 // a	∠ 2 ma ∠ 20µa
Current from DATA IN BIT 15 to Gnd 974 ma Current from 2.4V to DATA IN BIT 15 5.10 / a	
Current from DATA IN BIT 16 to Gnd -945 ma Current from 2.4V to DATA IN BIT 17 5.20 µa	≥ 2 ma ≤ 20 μa
Current from DATA IN BIT 17 to Gnd 950 ma Current from 2.4V to DATA IN BIT 17 5.32 NR	<u>اے</u> 2 ma <u>اے 20</u> 20

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^	ment Flactronics	Division

SIZE

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CODE IDENT NO. DWG NO. 94990

12-P13721D

8201 E. MCDOWELL ROAD SCOTISDALE, ARIZONA 85252

SCALE

REVISION

Date of Test 5-9-79 Tested By

Limit

7.6	VERIFICATION	OF	OPEN	COLLECTOR	ON	OUTPUT	SIGNALS

7.6.3 F	READ (COMPLETE	voltage	20	mv	Æ	100	mv
7.6.4 I	DATA (OUT BIT	0 voltage	25	mv	₩.	100	mv
	DATA (OUT BIT	1 voltage _	20	mv	ž.	100	mv
1	DATA (OUT BIT	2 voltage	20	mv	4	100	mv
1	DATA (OUT BIT	3 voltage	10	mv	٤.	100	mv
	DATA (OUT BIT	4 voltage	10	mv	±	100	mv
1	DATA (OUT BIT	5 voltage	10	mv	4	100	mv.
	DATA (OUT BIT	6 voltage	0	mv	¥	100	mv
	DATA (OUT BIT	7 voltage	0	mv	25	100	mv
1	DATA (OUT BIT	8 voltage	0	mv	\$	100	mv
	DATA (OUT BIT	9 voltage	10	mv	=	100	mv
	DATA (OUT BIT	10 voltage	25	mv	≝.	100	mv
	DATA (OUT BIT	11 voltage	30	mv	· =:	100	mv
	DATA (OUT BIT	12 voltage	25	mv	€:	100	mv-
	DATA (OUT BIT	13 voltage	30	mv	æ.	100	mv
	DATA	OUT BIT	14 voltage	30	mv	3.	100	mv
	DATA	OUT BIT	15 voltage	40	mv	€.	100	.mv
	DATA	OUT BIT	16 voltage	25	mv .	₹.	100	mv
	ATA	OUT BIT	17 voltage	30	mv	ببب	100	. mv

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GAVARE	mont	Clartrania	e Division

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SCALE

8/N	 4	<u> </u>
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Date of Test 5-9-75'
Tested By

Limits

7.7 POWER CONSUMPTION (25)	C	١

7.7.1 Memory +5V Voltage <u>5.011</u> Volts

Memory -6.1V voltage <u>6.102</u> Volts

+5V Current <u>10.5</u> ma

+5V Power <u>52.615</u> mw

7.7.2 Memory -6.1V Current 4.9 ma
Memory -6.1V Power 29.904 mw

7.7.3 Total Memory Idle Power 82.519 mw

7.7.5 Memory +5V Voltage 5.002 Volts
Memory -6.1V Voltage 6.100 Volts

+5V Current 690 ma +5V Power 3451.0 mw

7.7.6 Memory -6.1V Current <u>238</u> ma Memory -6.1V Power 1, 451.8 mw

7.7.7 Total Active Power 4902.8 mw

7.8 READ COMPLETE TIMING

7.8.5 Delay <u>410</u> ns

170 mw max

7000 mw max.

500 ns max. 250 ns min 450 ns m.x.



MOTOMOLA INC.

Government Electronics Division

8701 U. MCDOWELL ROAD SCOTSDALE, ARIZONA 85252 SIZE

CODE IDENT NO. DWG NO. 94990

12-P13721D

SCALE REVISION

ISTUET 30

- 400	11.00	
B/N	 13	

LIMITS

READ COMPLETE/DATA OUTPUT TIMING 7.8.7 7.8.8 OK REJECT DO-0 DO-1 OK REJECT OK REJECT DO-2 OK REJECT DO-3 OK DO-4 REJECT DO-5 OK REJECT OK REJECT DO-6 OK REJECT DO-7 OK DO-8 REJECT OK DO-9 REJECT OK DO-10 REJECT OK DO-11 REJECT DO-12 OK REJECT DO-13 OK REJECT DO-14 OK REJECT DO-15 OK REJECT OK DO-16 REJECT



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Government Electronics Division

DO-17

SIZE

94990

REJECT

12-P13721D

8201 E. McDOWELL ROAD
SCOTTSDALE, ARIZONA 85252 SCALE

OK

REVISION

CODE IDENT NO. DWG NO.

	S/N	103	, de la comanda	•	Date of Test	5-9-75
•	6.15			•	Tosted By	1
		• Samuel and the same		•		Limits
7.9	SYSTEM I	FUNCTIONAL TES	S T	•	• • • • • • • • • • • • • • • • • • •	
7.9.2		error occur?				
	No	-		•		and the second s
	Yes	_ Address	Bits			0 errors
7.9.4	Did an	error occur?		•		
•	No /		•			
	Yes	Address	Bits			0 errors
•				·		
.9.10		error occur?				en e
	No _	· ·				
	Yes	_ Address	Bits			0 errors
7.9.16	Did an	error occur?				
	No 🗸					
		Address	Bits			0 errors
	4.					
7.10	RANDOM	ACCESS CAPABII	31 TY			
7.10.6	Did an	error occur?				
	No ·	-	en jakor jakor Liikuva jakor j			
	Yes	Address	Bits			0 errors
7.10.7	Did an	error occur?				
	a) No					
	Yes	Address	Bits			0 errors
			•			
	DOM A	ILLE OF SIZE	CODE IDENT NO.	DWG NO.		

Government Electronics Division A 94990 12-P13721D

8701 E. MCDOW.C.L.L. ROAD
SCOTTSDALE, AMIZONA 85252 SCALE REVISION SHEET 32

	S/N 103	Date of Test 5-9-75
		Limits
•	b) No	
	Yes Address Bits	0 errors
	c) No	
	Yes Address Bits	0 errors
7.11	NON-VOLATILITY TEST	
7.11.7	Did an error occur?	
& 7.11.9	No	
	Ycs Address Bits	0 errors
7.12	MEMORY SELECT TEST	
7.12.3	Address OCCC (Octal)	0000
7.12.4	Address 0001 coop (Octal)	0000
	. 0010 0000 (Octal)	0000
	0011 0000 (Octal)	0000
	0100 <u>6000</u> (Octal)	0000
	0101 <u>00 co</u> (Octal)	0000
	0110 OCCO (Octal)	0000
	0111 OC CO (Octal)	0000
	1000 0000 (Octal)	0000
	1001 0000 (Octal)	0000
	1010 0000 (Octal)	0000
	[요. 10 10] 고향 보는 10 전 12 등이 되었다는 것으로 이 경기에 되었다. - 12 : 10 : 10 : 12 : 12 : 12 : 12 : 12 :	
	레일: B	. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1.

C. E.



MOTOROLA INC.	SIZE	CODE IDENT NO.	DWG NO.		
Government Electronics Division	Α	94990		12-P13721D	
8201 L. McDOWFLL ROAD SCOTTSDALE AUGUNA 85252	COALC	lactic	<u> </u>		

	S/N 103	Date of Test 5-9-75	
		Tested By	
		<u>Limits</u>	heacters.
•	Address 1011 6000 (Octal)	0000	
	1100 0000 (Octal)	0000	and the second
	1101 <u>0000</u> (Octal)	0000	Ţ
	1110 <u>0000</u> (Octal)	0000	L
7 10 B	Did an error occur?		ſ
7,12,0	No /		L
	Yos Address Bits	0 errors	
7.13	WORST CASE PATTERN TEST		
7 13 2	Did an error occur?		~~
	No ~		
	Yes Address Bits	0 errors	51
7.13.3	Did an error occur?		i Marien
	No	등 설레이트 등 보고 있는 그 같은 사람들은 사람들은 함께 보고 있다. 사람들은 사람들은 기를 보고 있는 것이 되었다.	J
	Yes Address Bits	0 errors	T
	사용 등에 발표 전에 보고 있는 것이 되었다. 보고 있는 기계 기계 등에 발표하는 것이 있는데 있는 것을 했다.		لبة
			j
			()
			U
			[]
	그렇게 하고 싶다면 가장이 하면 하는데 그는 사람이 하게 하게 되었다. 그렇게 하고 말하는데 하는데 하는 것 같은 그런데 하는데 하는데 하는데 하는데 보다 하게 하는데 하는데 하는데 하는데 되었다. 그는데 말하는데 말하는데 되었다.	일이 되는 현실하게 하고 하면 물론이 되는 때는 경찰이나 및 경험을 보였다. 그는 발표 마이트를 하게 했다. 그 나는 그들이 하라고 있는 것이 없다는 모든 것이다.	IJ
			A TOP AND A TOP A
	보다 보고 있다. 이번 경기 사람들은 보고 있는 사람들은 것이 되었다. 1일 1일 : 이번 전 1일		
	- Leize Loope income	NO TOWO NO	
MOTO	TOLA INC. SIZE CODE IDENTI		
	Electronics Division A 94990	12-P13721D	
10110 22	E. MCDOWELL ROAD DALE, ANDZONA 85252 SCALE RE	VISION SHEET 34	-

	S/N	103			Date of To	(
3.4	a)		error occur?			Limits
			Address	Bit		0 errors
	b)	No _/	error occur?			
		Yes	Address	Bit		0 errors

Government Electronics Division

A 94990

SIZE

12-P13721D

CODE IDENT NO. DWG NO.

UIII PLATED WIRE MEDICEY 4601-400 5-5-75 CENTROL 41 10.0.3039 HIGH VACUUM TEST Vacuum System No. PRESSURE (mm Hg A) REMARKS TIME START To H. Unc 1030 LYXD" 3.1×10 1230 1x10 1300 127110-12 1330 8.8×10-6 1340 8,6xi0 VENT TO AMBO OPEN BILL JAK- END TEST PRECEDING PAGE BLANK NOT ET MEI Page

MOTOROLA/GED KO166 1/69

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TYPE OF												_		T NO.	_	•			PTION	- 7		
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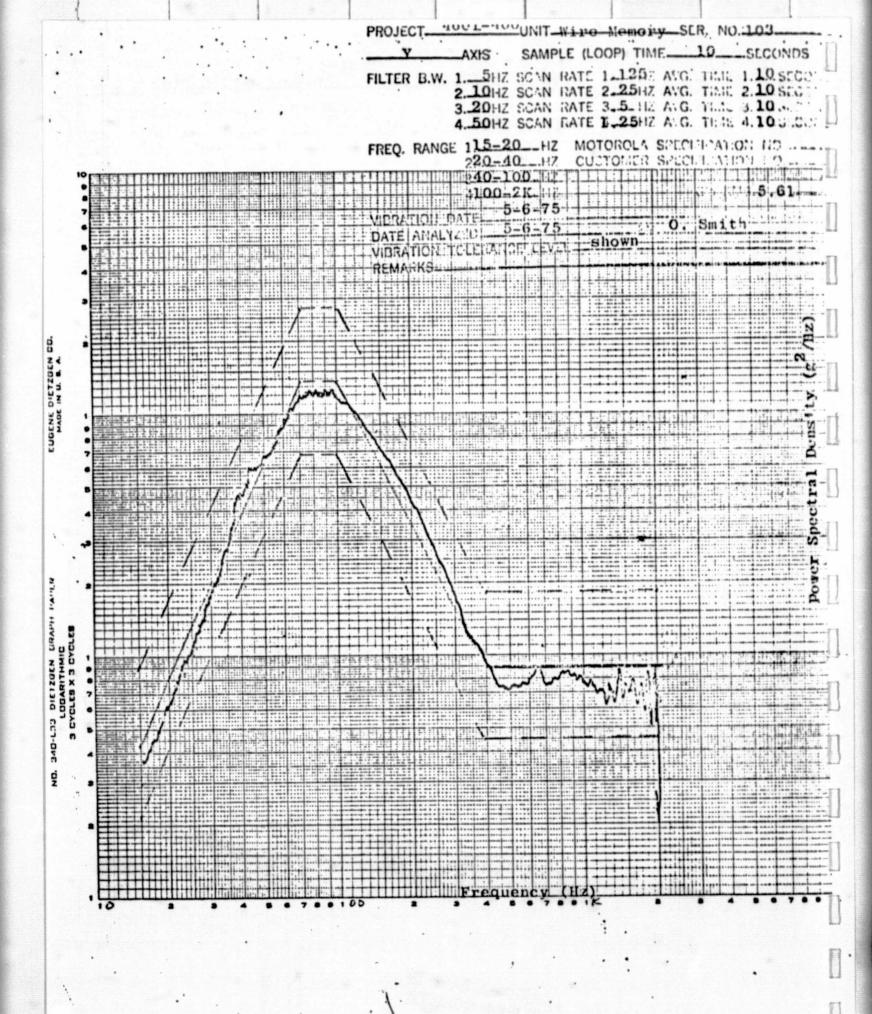
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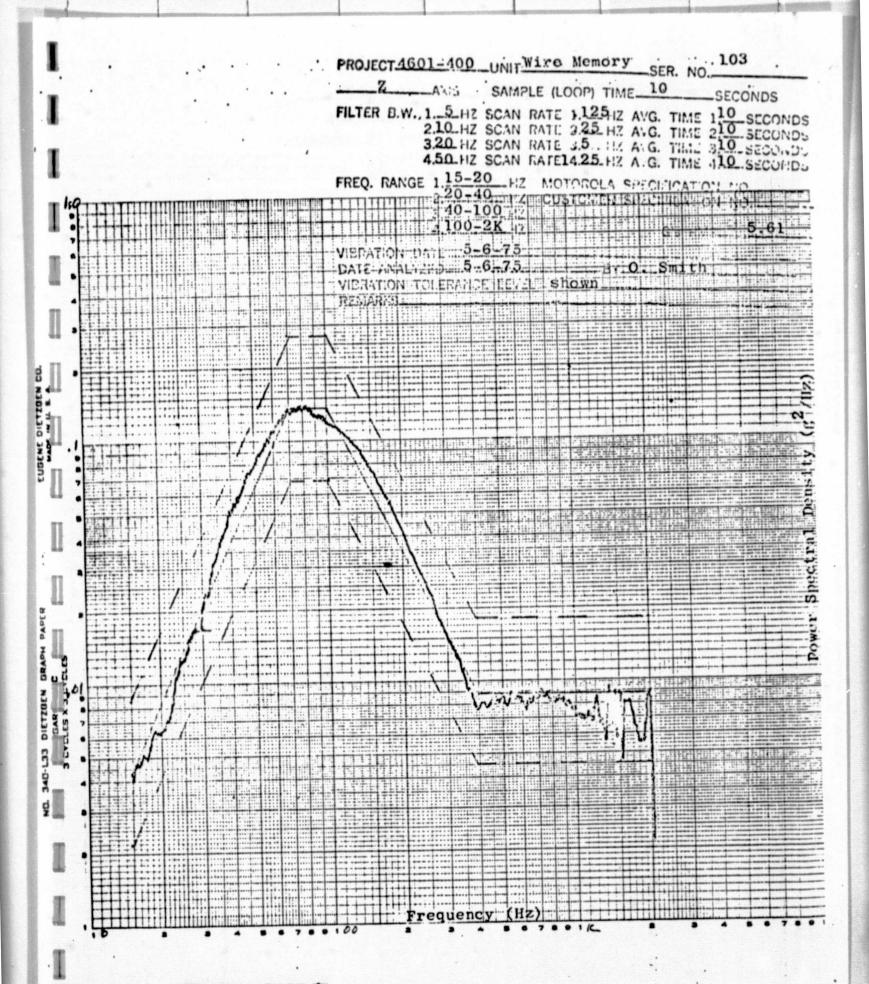
MOTOROLA INC.	VIBRATION TEST	· \ X
SHEET	UNIT PLATED WIRE MEMORY	* 1
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SPEC DETAILS 12-	-P13722 D	X/TY

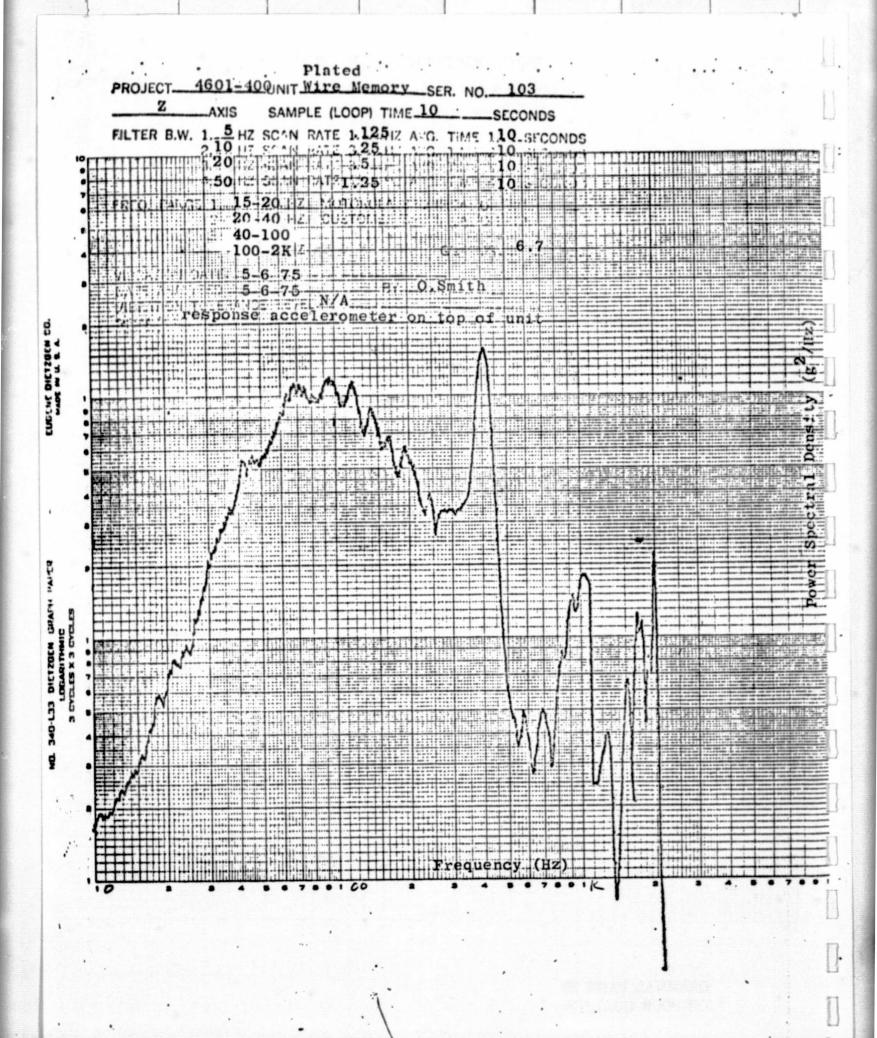
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RUN NO	START	STOP	VIB. TIME	NO.	D.A.	G'S MV (RMS)			
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7/2	1901	1901	20586	103	NA	5,61	16		11
2/3	1938	1938	LOSEC	103	NA	5.61	"("	. ((
3/4	1954	1958	421	103	., 33"	10-5	5-2K1	12	
X 5	2111		2 min	107	MA		SHAPED	RANDON	NOISE
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1	2148		105CC	103	44		SHAPEO	RANDON	NOISE
E	2248	2/52	421	103	.33"	70,7-15.3	5-2KH	2	
4	2157	2259	2 Min	103	NA	5.61 50.1	SHAPED	RANDOM	NOISE
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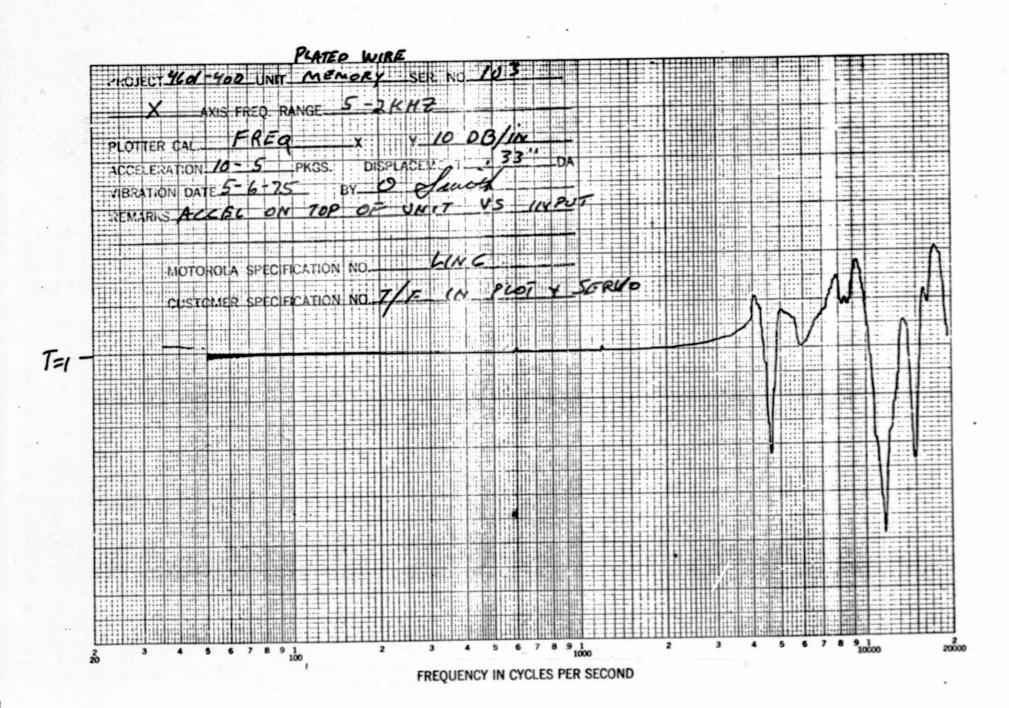
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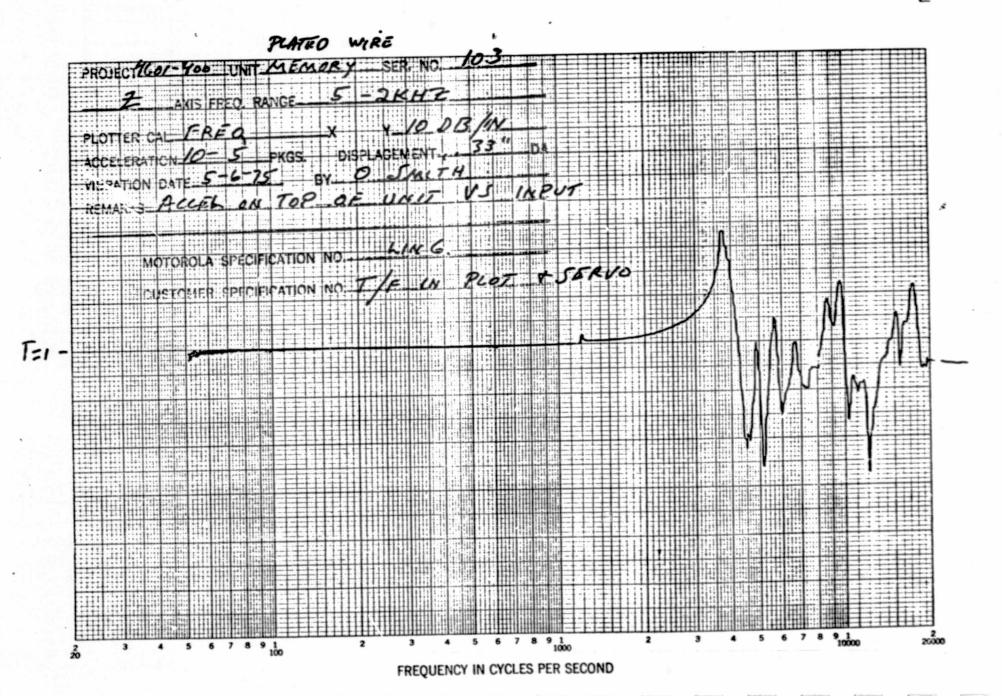






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ATTACHMENT III

ACCEPTANCE TEST DATA SHEET,

LOW POWER RANDOM ACCESS SP

SPACECRAFT MEMORY

PART NO. 12-P13721D

DRAWING NO. 12+P13721D

SERIAL NUMBER 104

(35 PAGES)

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HEV N2 X4 SHEET 27 2	8 29 30	31 3	2 33 (1 X1	34 X1	35					X1 X 14 1		_								1.
HEV N2 X4 SHEET 27 2	8 29 30 REV x 5 EET 1	31 3 x5 x	2 33 (1 X1	34 X1	35 X1 X1							_								1.
NEV 87 X- FIGET 87 26 EV STATUS R OF SHEETS SH	8 29 30 EEV x 5 EET 1	31 3 x5 x 2 3	12 33 (1 X) 1 4	34 X1 5	35 X1 X1 6 7	8	9 1	0 11 1				_								1.
MEV %2 X- FIEET R7 2 EV STATUS R OF SHEETS SH OR ASSOCIATED LI INTERPRET DRAWIN	8 29 30 REV x 5 EET 1 ISTS SEE G IN ACCOR	31 3 x5 x 2 3	2 33 (1 X1 3 4	34 X1 5	35 X1 X1 6 7	8	9 1	0 1 1 1 BY	2 13	14 1	5 16	17	18	19 20	2:	1 22	23	24	25	26
MEV 32 X- SHEET 27 2 EV STATUS R OF SHEETS SH OR ASSOCIATED LI INTERPRET DRAWIN INLESS OTHERWISE ALL DIMERSIONS	8 29 30 REV x 5 EET 1 ISTS SEE G IN ACCOR SPECIFIED ARE IN	31 3 x5 x 2 3	82 33 K1 X1 B 4 E WITH	34 X1 5	35 X1 X1 6 7	8	9 1	0 1 1 1 BY	2 13	14 1	5 16	17 NC	18		EAS	1 22 T Mc	DOW	24 ELL	25 ROA	26 D
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MEV 32 X- SHEET 27 2 EV STATUS R OF SHEETS SH OR ASSOCIATED LI INTERPRET DRAWIN INLESS CTHERWISE ALL DIMERSIONS ENCHES AND END	8 29 30 REV x 5 EET 1 ISTS SEE G IN ACCOR SPECIFIED ARE IN USE, FOR	31 3 x5 x 2 3 RDANCI DR BY CHK E	E WITH H H N N N N N N N N N N N N N N N N N	34 X1 5 STAIR	35 X1 X1 6 7 7 7 7 7 7 7 7 7 7	PRESC 4339 4601	9 1	0 1 1 1 BY	PO ACC LOW	ROL Electro	5 16 A Price C	NO TES	on /	/ 8201 SCOT	EAS TSC	T Mc	DOWI , ARI	ELL IZON	ROA A 85	26 D
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EV STATUS R OF SHEETS SH OR ASSOCIATED LI INTERPRET DRAWIN INLESS OTHERWISE ALL DIMERSIONS (ECHES AND END INTERPRET SHEET) TOLERANCES SE	8 29 30 REV x 5 EET 1 ISTS SEE G IN ACCOR SPECIFIED ARE IN USE, FOR	31 3 x5 x 2 3 DANCI DR BY CHK E AFG CONTINUAL	E WITH H H N N N N N N N N N N N N N N N N N	34 X1 5 STAN	35 X1 X1 6 7 DARDS Ceed PROJUD. 2316 2057	PRESC 4339 4601 3 6	9 1	BY SIZE	POP	POLE POWER MENT AND	A I I NO.	NO Oivision TES	on /	/ 8201 SCOT DATA ACC RT N	EAS TSE SI ESS O.	T Mc	DOWI , ARI PAC	ELL ZON E- 370	ROA A 85	26 D
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1. SCOPE This test data sheet is to be used to record data as required by the Acceptance Test Procedure for the Low Power Random Access Spacecraft Memory. 2. REFERENCE INFORMATION SPECIFICATIONS APPLICABLE 2.1 8-562-P 3 Low Power Random Access Spacecraft Memory 12-P13722D Acceptance Test Procedure, Low Power Random Access Spacecraft Memory TEST DATA 3. Unit 8/N 104 Start Date of Tests Tested by ATP PARA. NO. 3.1 EQUIVALENT TEST EQUIPMENT DC Millioneter H.P 428A 0-1A Digital Volt meter Fluke 8120A (Multimeter) Counter

PHYSICAL CHARACTERISTICS

Limit



6.1 WEIGHT

Weight of LP-RASM = 5.562 Pounds

6.5 pounds (aluminum)

5.8 pounds (magnesium)

MOTOROLA INC.
Government Electronics Division

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94990

12- P13721D

8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252 SCALE

SIZE

REVISION

CODE IDENT NO. DWG NO.

8/N 104

Date of Test 5/26/75

6.2 DIMENSIONS

Limit

H = 2.895 inches

 $W = \frac{6.63c}{1000}$ inches

MW= 8.955 inches

 $D = \frac{1}{2} \cdot 322$ inches

MD- _____ inches

 $V = H \times W \times D = 157.i-i$ inches³

≤ 160 inches³

WOTOROLA INC.
Government Electronics Division

8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252 SIZE

SCALE

CODE IDENT NO. DWG NO.

A 94990

12-P13721D

REVISION

SHEET

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/N	104		Date of Test	5/28/75
			Testod By	
		•		

7.4	CHASSIS ISOLATION	Limit
	Impedance 29 meg 1	≥ 9 megohm
7.5	INPUT SIGNAL LOADING	
7.5.2	Current from INITIATE PULSE to Gnd 1,405ma /	≤ 2 ma
	Current from 2.4V to INITIATE PULSE 1.40 pa	≤ 20 µa
7.5.3	Current from MEM SEL 1 to Gnd 1.463 ma	, ≤ 2 ma
	Current from 2.4V to MEM SEL 1	≤ 20 µ a
7.5.4	Current from MEM SEL 2 to Gnd 1,407 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 2 1.41 ya	≤ 20 µa
	Current from MEM SEL 3 to Gnd 1,408 ma	≤ 2 ma
	Current from 2.4V to MEL SEL 3 1,42 ya	≤ 20 µ a
	Current from MEM SEL 4 to Gndma	≤ 2 ma
	Current from 2.4V to MEM SEL 4 1.02 ya	≤20 µa
7.5.5	Current from READ/WRITE to Gnd 1,008 ma	≤ 2 ma
	Current from 2.4V to READ/WRITE 1,30 ya	≥ 20 µa
7.5.6	Current from ADDRESS 20 to Gnd	≤ 2 ma
	Current from 2.4V to ADDRESS 20 5.62 pa	≤20 µa
	경기가 된 경기를 하는 사람들은 이 얼마를 살고 있는 하다면 되는 것이다. 그리다 모임자	

MOTOROLA INC.
Government Electronics Division

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94990

12-P13721D

8701 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

SCALE

SIZE

REVISION

CODE IDENT NO. DWG NO.

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Date of Test 5/28/75

Tested By

4	•		Limits
Current	f: om ADDRESS	2 to Gnd	≤ 2 ma
Current	from 2.4V to	ADDRESS 21 6/7 pa	≤ 20 µa
Current	from ADDRESS	2 ² to Gnd	≤ 2 ma
Current	from 2.4V to	Address $2^2 7.06 \mu a$	≤20 µ a
		2 ³ to Gnd	, \$ 2 ma
Current	from 2.4V to	Address 23 7,80 pa	≤ 20 _µ a
		24 to Gnd	≤ 2 ma
Current	from 2.4V to	ADDRESS 24 8,22 pa	€ 20 µa





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Government Electronics Division

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CODE IDENT NO. DWG NO. 94990

12-P13721D

8701 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

SCALE

SIZE

REVISION

SHEET

5

8/N 104

Date of Test 5/28/75
Tested By

		·	_			Li	mits	. !
Current	from	ADDRESS	2 ⁵ to Gnd	,906	ma	₹	2 ma	
Current	from	2.4V to	ADDRESS 2 ⁵	5,69	μa	≟ 2	ONA	
Current	from	ADDRESS	2 ⁶ to Gnd	1901	_ ma	4	2 ma	1
Current	from	2.4V to	ADDRESS 2 ⁵	5,79	μa	<u></u>	20 <i>ju</i> a	

	A CONTRACT OF THE STATE OF THE
Current from ADDRESS 27 to Gnd	<u>173</u> ma <u>≤</u> 2 ma
Current from 2.4V to ADDRESS 27	12 pa < 20 pa
Current from ADDRESS 28 to Gnd	146 ma = 2 ma
Current from 2.4V to ADDRESS 28 /	
Current from ADDRESS 29 to Gnd	935 ma 4.2 ma
Current from 2.4V to ADDRESS 29 /,	
Current from ADDRESS 2 to Gnd /	006 ma \(\preceq 2 ma
Current from 2.4V to ADDRESS 210	
Current from ADDRESS 2 ¹¹ to Gnd/	,008 ma ≤ 2 ma
Current from 2.4V to ADDRESS 211	1,36 µa = 20 µa
Current from DATA IN BIT 0 to Gnd	1,061 ma = 2 ma
Current from 2.4V to DATA IN BIT 0	化机械 化二氢化二十二甲二甲基 化二氯甲基甲基甲基甲基甲基甲基甲基甲基甲基甲基甲基甲基甲基甲基甲基甲基甲基甲基甲基
	电热点重新 电抗工作 医有线 医电流流 人名西葡克克 化二烷



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MOTOROLA INC.

Government Electronics Division

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SIZE

94990

12-P13721D

8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

SCALE

REVISION

CODE IDENT NO. DWG NO.

			•	•	Limits
Currer	nt from	DATA II	N BIT 1 to Gnd	1.672 ma	≤ 2 ma
			DATA IN BIT 1	_ ~	≥ 20 Na
Currer	it from	DATA II	N BIT 2 to Gnd	1,08 (ma	≤ 2 ma
			DATA IN BIT 2		£ 20µ a
Currer	at from	DATA II	N BIT 3 to Gnd	1.045 ma	<u>≼</u> 2 ma
			DATA IN BIT 3		∠ 20/Va
				,	
Currer	nt from	DATA I	N BIT 4 to Gnd	1,03/ ma	∠ 2 ma
Curren	nt from	2.4V t	DATA IN BIT 4	9.62 Ma	€ 20×2
Curre	nt from	DATA I	N BIT 5 to Gnd	1,052 ma	≤ 2 ma
			DATA IN BIT 5		ع در 20 <u>م</u>
				·	
Curre	nt from	DATA I	N BIT 6 to Gnd	1.073 ma	≤ 2 ma
Curre	nt from	2.4V t	DATA IN BIT 6	7.88 pa	€20/Ja
Curre	nt from	DATA I	N BIT 7 to Gnd	1,057 ma	∠ 2 ma
			o DATA IN BIT 7		<u>∠</u> 20µa
Curre	nt from	DATA I	N BIT 8 to Gnd	1,05/ ma	∠ 2 ma
Curre	nt from	2.4V t	o DATA IN BIT 8	8.11 pa	₹20µa
Curre	nt from	DATA I	N BIT 9 to Gnd	,99/ ma	<u></u> 4 2 ma
			o DATA IN BIT 9		عر 20 ×
, , , , , , , , , , , , , , , , , , ,					





MOTOROLA INC.	SIZE	CODE IDENT NO.	DWG NO.
Government Electronics Division	Α	94990	

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i. Villa Silvati	•	Limits
Current from DATA	IN BIT 10 to Gnd	<u>∠</u> 2 ma
and the property of the control of t	to DATA IN BIT 10 9.3/pa	£ 20/12
Current from DATA	IN BIT 11 to Gnd	4 2 ma
Current from 2.4V	to DATA IN BIT 11 84/ pa	£ 20/0 a
Current from DATA	IN BIT 12 to Gnd 1,053 ma	<u></u> 2 ma
Current from 2.4V	to DATA IN BIT 12 _ 9,86 µa	£ 20 µ 2
Current from DATA	IN BIT 13 to Gnd	∠ 2 ma
	to DATA IN BIT 14 9,53 µa	< 20 µa
	A 7A	
	IN BIT 14 to Gnd	∠ 2 ma
Current from 2.4V	to DATA IN BIT 14 9,27 µ a	عر20 کے
Current from DATA	IN BIT 15 to Gnd 1,056 ma	
	to DATA IN BIT 15 6.3/ Na	≤ 20µa
	IN BIT 16 to Gnd 1040 ma	<u>2</u> 2 ma
Current from 2.4V	to DATA IN BIT 17 6.43 Na	= 20 µa
Current from DATA	IN BIT 17 to Gnd	<u>∠</u> 2 ma
	to DATA IN BIT 17 7.57 NR	4 20 pa
그림 그는 이를 생각하는 것은 이번들에 살았다.		현실 그 기가 가게 되었다.





MO	70	MOL	4 /	NC.
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Date of Test 5/28 Tested By

Limit

7.6	VERIFICATION OF OPEN COL	LECTOR ON	OUTPUT	SIGNALS	
7.6.3	READ COMPLETE voltage	50	mv		≤ 100 mv
7.6.4	DATA OUT BIT 0 voltage	20	mv		≤ 100 mv
	DATA OUT BIT 1 voltage	20	mv		≾ 100 mv
	DATA OUT BIT 2 voltage _	10	mv .		≤ 100 mv
	DATA OUT BIT 3 voltage	QO	mv		≤ 100 mv
	DATA OUT BIT 4 voltage	10	mv		≤ 100 mv
	DATA OUT BIT 5 voltage	0	mv		≤ 100 mv
	DATA OUT BIT 6 voltage	10	mv		≤ 100 mv
	DATA OUT BIT 7 voltage	0	mv		= 100 mv
	DATA OUT BIT 8 voltage _	0	mv		≤ 100 mv
	DATA OUT BIT 9 voltage	20	mv		≤ 100 mv
	DATA OUT BIT 10 voltage	20	mv		≤ 100·mv
	DATA OUT BIT 11 voltage	20	mv		≤ 100 mv
	DATA OUT BIT 12 voltage	20	mv		≤ 100 mv
	DATA OUT BIT 13 voltage	25	mv		≤ 100 mv
	DATA OUT BIT 14 voltage	40	ΜV		< 100 mv
	DATA OUT BIT 15 voltage	10	mv		≤ 100 mv
	DATA OUT BIT 16 voltage	10	mv		100 mv
	DATA OUT BIT 17 voltage		mv		≤ 100 my





MOTO	ROLA	INC.
Government	Flactronics	Division

94990

12-P13721D

8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

SCALE

SIZE

REVISION

CODE IDENT NO. DWG NO.

	s/n 104			st 5/28/79
			Tested By	124-11
				Limits
7.7.1.	POWER CONSUMPTION (25°C)	•		
7.7.1	Memory +5V Voltage 5,005 V			
	Memory -6.1V voltage 4,103 V	olts		
	+5V Current	a		
•	+5V Power <u>50.5505</u> m	W	: <i>t</i>	
7.7.2	Memory -6.1V Current 3.15 m	8.		
	Memory -6.1V Power 19,22445 m	w '		
7.7.3	Total Memory Idle Power (9.77475 m	w		170 mw max
7.7.5	Memory +5V Voltage <u>5.001</u> V	olts		
	Memory -6.1V Voltage 4,105 V	olts		
	+5V Current 665 m	a		
	+5V Power <u>3325,465</u> m	w		
7.7.6	Memory -6.1V Current 225 m	a		
1 at 1 m m of N	Memory -6.1V Power 1373.625 m	w		
7.7.7	Total Active Power 4699,290 m	w		7000 mw max.
7.8	READ COMPLETE TIMING			
7.8.5	Dolay 395 ns			500 ns max.
	Duration 320 ns			250 ns min
				450 ns max.
nan-re	SIZE CODE IDENT	NO. DWG NO.		

SHEET SCALE REVISION

12-P13721D

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94990

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MOTOROLA INC.

Government Electronics Division

8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

8/1	N	•		Date of Tes	55
7.8.7	READ CO	MPLETI	E/DATA OUTPUT TIN	AING	LIMITS
7.8.8	DO- 0	OK	REJECT		
	DO-1	ок	REJECT_		•
	DO-2	OK	REJECT	en e	en de la proposición de la companya de la companya La companya de la co
	DO-3	OK_	REJECT		
	DO-4	OK	REJECT		
	DO-5	OK_	REJECT		
	DO-6	OK	REJECT		
	DO-7	OK_	REJECT		REFER
	DO-8	OK_	REJECT		TEST P
	DO-9	OK_	REJECT		
	DO-10	OK_	REJECT		
	DO-11	OK_	REJECT		
	DO-12	ок_	REJECT		
	DO-13	OK_	REJECT		
	DO-14	OK_	REJECT_		
L	DO-15	OK_	REJECT_		
	DO-16	OK_	REJECT		
	DO-17	OK_	REJECT		





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1	MOTOROLA INC.	SIZE	CODE IDENT NO.	DWG NO.				
7.00	Government Electronics Division	Α	94990		12-P13721D) i		*
100	8701 E. McDOWELL ROAD		•	<u> </u>				
*	SCOTTSDALE, ARIZONA 85252	SCALE	REVIS	ION -	S	SHEET	11	

	s/N		Date of Tes Tested By	5/28/74
	en de la companya de La companya de la co		.	Limits
7.9	SYSTEM FUNCTIONAL TEST			
7.9.2	Did an error occur?			
	NoX			•
	Yes Address	Bits		0 errors
7.9.4	Did an error occur?			
	No X			
	Yes Address	Bits		0 errors
7.9.10	Did an error occur?			
	No <u>X</u> _			
v van	Yes Address	Bits		0 errors
7.9.16	Did an error occur?			
	No X			
	Yes Address	Bits		0 errors
7.10	RANDOM ACCESS CAPABILI	TY		
7.10.6	Did an error occur?			
	No X			
	Yes Address	Bits		0 errors
7.10.7	Did an error occur?			
	a) No X			
	Yes Address	Bits		0 errors
MOTO	ROLA INC. SIZE	CODE IDENT NO. DWG NO.		

Government Electronics Division A 94990 12-P13721D

8701 E. McDOWILL ROAD SCOTISDALE, ARIZONA 85252 SCALE REVISION SHEET 12

	s/n	104	•		Date of Test	5/28/75
					Tested By	Limits
	b) No Yes		ress	Bits		0 errors
	c) No Yes			Bits		0 errors
.11	NON-VOL	ATILITY TEST				
0_	Did an	error occur?				
	Yes	_ Address _	Bits	•		0 errors
.12	MEMORY	SELECT TEST	*			
.12.3	Address	0000 (00	tal)			0000
.12.4	Address	0001 0000	(Octal)			0000
		0010 0000				9000
		0011 0000	•			0000
		0100 0000				. 0000
		0101 <u>0000</u> 0110 0000				0000
		0110 <u>0000</u>				0000
		1000 <u>0000</u>				0000
		1001 0000	•			0000
		1010 0000				0000





1	TOTOROLA INC.	SIZE	CODE IDENT NO.	DWG NO.			
	vernment Electronics Division		94990		12-P13721D		
W.	8201 E. McDOWELL ROAD	L					
	SCOTTSDALE, ARIZONA 85252	SCALE	REVIS	ION	SHEET	13	

	s/n <u>104</u>	Date o	f Test 5/28/
1		Tested	By Zamila
To come to com			Limits
6	Address 1011 0000 (Octal)	• * • • • • • • • • • • • • • • • • • •	0000
	1100 0000 (Octal)		0000
	1101 0000 (Octal)		0000
	1110 0000 (Octal)		0000
12.6	Did an error occur?		•
	No _X		
	Yes Address Bits _		0 errors
10	WORST CASE PATTERN TEST		
.13	WORST CASE PATIENT TEST		
.13.2	Did an error occur?		
	No X		
	Yes Address Bits		0 errore
.13.3	Did an error occur?		
	No X		
	Yes Address Bits		0 errors
	성으로 보고 있습니다. 그런데 그를 보고 있습니다. 그런데		
	경기 등 경기 등 경기 등 경기 등 경기 등 등 경기 등 등 등 경기 등 등 등 경기 등 등 등 기계 등 경기 등 경기		된 : 2010년 - 1212년 - 1222년 - 1 1222년 - 1222년
		요 . 그리고 하고 하고 있다고 있다. 글로 그 맛이 보고 낡아 이 해 다니다.	

Government Electronics Division

94990

12-P13721D

8701 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

SCALE

SIZE

REVISION

CODE IDENT NO. DWG NO.

	s/n		104			ite of Test ested By	4.11.
	*		•		•		Limits
13.4	a)	Did	an error occi	ur?			
		No	<u> </u>	•			
		Yes	Address	sBit			0 errors
	b)	7 1.4	an error occi				.
		No	X	ur r			
		Yes	Áddres	s Bit			0 errors
							•





25								
١.	111	-	-	-	MO			
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E#	11				JANS H A	1	# # U.T	14 m
23	v		_					
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Government Electronics Division

8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252 n A

SIZE

94990

CODE IDENT NO. DWG NO.

12-P13721D

SCALE REVISION SHEET 15

5/N	DATE OF TEST 5/29/75 TESTED BY
8.	TEMPERATURE TEST
8.2.1	TIME 7:00
8.2.2	LOW TEMPERATURE
	THERMISTOR RESISTANCE 150 MINUTES <u>200</u> K OHMS
	160 MINUTES 204 K OHMS % CHANGE 2%
	170 MINUTES K OHMS % CHANGE 180 MINUTES K OHMS % CHANGE
	190 MINUTES K OHMS % CHANGE
8.2.3	DID AN ERROR OCCUR?
	YES ADDRESS BITS 0 ERRORS
8.2.4	-6.1 v voltage 6.404 volts +5 v voltage 5.249 volts
	-6.1 V CURRENT 14.0 ma +5 V CURRENT 10.8 ma -6.1 V POWER 89.656 mw +5 V POWER 56.6892 mw
	TOTAL MEMORY IDLE POWER 146,3452mw 170 mw MAX
8.2,5	-6.1 V VOLTAGE (.40) VOLTS +5 V VOLTAGE 5.249 VOLTS
	-6.1 V CURRENT 254 ma +5 V CURRENT 685 ma -6.1 V POWER /62565 mw +5 V POWER 3395565 mw
	L CLIZE I CODE IDENT NO TOWO NO
	Electronics Division A 94990 12-P13721D
	ST McDOWELL ROAD OALE, ARIZONA 85257 SCALE REVISION SHEET 16

s/N	104		DATE OF	TEST 5/2 9/75
			TESTED	BY 29
	•			LIMITS
8.2.6	DID AN EA	ROR OCCUR?		
	NO X			
	YES	ADDRESS	BIT	0 ERRORS
8.2.8	WC a) DI	D AN ERROR OCCUR?		
	ио 🗡	·		
	YES	ADDRESS	BIT	0 ERRORS
	WC b) DID	AN ERROR OCCUR?		
	NO X			
	YES	ADDRESS	BIT	0 ERRORS
	WC c) DID	AN ERROR OCCUR?		
	NO X			
	YES	ADDRESS	BIT	0 ERRORS
		AN ERROR OCCUR?		
	NO X			
	YES	ADDRESS	BIT	O ERRORS
8.2.11	WC a) DID	AN ERROR OCCUR?		
	NO X			
	YES	ADDRESS	віт	O ERRORS

7	•				-	in a		٨	C I		ندنده		- 0		
SALES SALES	l	V	1	C)	7	C	0/	1	C	L	A	1	N	C

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SCALE

CODE IDENT NO.

94990

12-P13721D

8701 EAST MCDOWELL ROAD SCOTTSDALE, ARIZONA 85257

REVISION

s/N	104	DATE OF TEST	5/29/76
		TESTED BY	LIMITS
8,2,11	(Cont.)		**************************************
	WC b) DID AN ERROR OCCUR?		
	YES ADDRESS	BIT	O ERRORS
	WC c) DID AN ERROR OCCUR?		
	YES ADDRESS	BIT	O ERRORS
	WC d) DID AN ERROR OCCUR?		
	YES ADDRESS	BIT	
8.3	INTERMEDIATE TEMPERATURE TEST		
	TIME 10:16		
8.3.2	The same of the sa	NO X YES	O ERRORS
	11:06 34.3 K OHMS 11:06 11.6 K OHMS	NO X YES NO X YES NO YES NO YES	O ERRORS O ERRORS O ERRORS
	11:36 4 K OHMS 11:36 3,4/ K OHMS	NO Y YES NO X YES NO Y YES NO Y YES	O ERRORS O ERRORS O ERRORS
	11:56 2.04 K OHMS 12:06 1.71 K OHMS	NO X YES NO X YES NO YES NO YES	O ERRORS O ERRORS O ERRORS
	ROLA INC. SIZE CODE IDENT N Electronics Division A 94990	10. DWG NO.	

REVISION

SCALE

SHEET

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8201 EAST McDOWELL ROAD SCOTTSDALE, ARIZONA 85257

s/n	104
	TESTED BY
	LIMITS
8.3.3	TIME
8.4	50 MINUTES K OHMS
	60 MINUTES K OHMS % CHANGE
	70 MINUTES K OHMS % CHANGE
	80 MINUTES 1.51 K OHMS % CHANGE
	90 MINUTES 1.61 K OHMS % CHANGE .000%.
8.4.1	-6.1 V VOLTAGE 6.403 VOLTS +5 V VOLTAGE 5.256 VOLTS
	-6.1 V CURRENT 7.1 ma +5 V CURRENT 12.0ma
	-6.1 V POWER 45.4413 mw +5 V POWER 63.072 mw
	TOTAL MEMORY IDLE POWER 105.5333 mw 170 mw MAX
8.4.2	DID AN ERROR OCCUR?
	NO X
	YES ADDRESS BIT O ERRORS
8.4.3	-6.1 V VOLTAGE 6.400 VOLTS +5 V VOLTAGE 5.258 VOLTS
	-6.1 V CURRENT 275 ma +5 V VOLTAGE 790 ma
	-6.1 V POWER 756.0 mw 1760 +5 V POWER 4053.52 mw 415282
	TOTAL MEMORY OPERATING POWER 6003,72 mw 7000 mw MAX
8.4.4	WC a) DID AN ERROR OCCUR?
	YES ADDRESS BIT O ERRORS
	SIZE CODE IDENT NO. DWG NO.
GOTO.	"VOLA IVO.
	ST McDOWELL ROAD A 94990 12-P13721D
	DALE, ARIZONA 85257 SCALE REVISION SHEET 19

SHEET

. s/N	104	• • • • • • • • • • • • • • • • • • •	DATE OF TE	ST 5/29/75
			TESTED BY	A Frankli
8.4.4	(Cont.)			LIMITS
	WC b) DID AN E	RROR OCCUR?		
	NO X			46.6
	YES	ADDRESS	BIT	O ERRORS
	WC c) DID AN E	ERROR OCCUR?		
	NO X			
	YES	ADDRESS	BIT'	O ERRORS
	WC d) DID AN E	ERROR OCCUR ?		
	NO X			
		ADDRESS	BIT	O ERRORS
8.4.6	WC a) DID AN I	ERROR OCCUR?		
	NO X	ADDRESS	BIT	O ERRORS
	WC b) DID AN I	ERROR OCCUR?		
	NO X YES	ADDRESS	BIT	O ERRORS
	WC c) DID AN I	ERROR OCCUR?		
	NO X YES	ADDRESS	BIT	O ERRORS
	WC d) DID AN I	ERROR OCCUR?		
	NO X	ADDRESS	BIT	O ERRORS
8.4.7	DID AN ERROR	OCCUR?		
	мо <u>X</u>	12. * - 12 - 12 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		
	YES	ADDRESS	BIT	O ERRORS
	ROLA INC			() () () () () () () () () ()
8701 EAS	ST McDOWELL ROAD DALE, ARIZONA 85257	-	12-P	13721D SHEET 20

	8/N 101			est <u>L.3 75</u>	
		•	Tested by	Fin like	
		•	•	•	
	TA CYULL MEGIN		• *	Limits	(B)
9.2	VACUUM TEST Did Any Bit Erro	ong Occur?		• • • • • • • • • • • • • • • • • • •	a 1075
	No L	ors occurr			Juil 3 1975
	Yos Addres	ss Bits		0 Errors	
1					
9.2.1	Fast Decompress:	ion	(): ()		
	Date (3-75	Tested	by Fin	the same	
	Did Any Bit Erre	ors Occur?			
	No				
	YesAddr	essBlt	S	0 Errors	
9.2.2	Hard Vacuum			~ ^	
	Date 6.3-75	Tested	by Ju	Tell-	
	Did Any Bit Err	ors Occur?			
	No_L				
	Yes	Address	Bits	0 Errors	11111 3 1975
10.	VIBRATION TEST			ΔΛ	
	Date (2.5.");	Tested	by Att	<u>Jela</u>	51975
	SINE SWEEP				®
	Axis X - Did An	y Bit Errors Oc	cur?		
	No 4				
	Yes Fre	q Address	Bits	0 Errors	
		naur ess			
	TULA ING.	SIZE CODE IDENT N			
~	Electronics Division	A 94990	1	2-P13721D	
SCOTTSD/	MCDOWELL ROAD ALE, ARIZONA 85252	SCALE RE	VISION	SHEE	T 21
AM 2 0 1000 1004.2.					

	8/N 104	i^{\prime}	Date of Test	5-7-00	The state of the s
	Axis Y - Did Any B	it Error Occur		Limits 334 6	8
	Yes Freq	Address	Bits	0 Errors	
	Axis Z - Did Any I	Bit Errors Occu	r?		
	Yes Freq	Address	Bits	0 Errors	
	RANDOM VIBRATION				
	Axis X - Did Any I	Bit Errors Occu	r?		
	Yes Freq	entre de la companya		0 Errors	
	Axis Y - Did Any I	Bit Errors Occu			X, Months (1)
	Ycs Freq	Address	`Bits	0 Errors	
	Axis Z - Did Any I	Bit Errors Occu	r?		
	Yes Freq	Address	Bits	o Errors	511
11.	SHOCK TEST				
	Date <u>5.30.75</u> 6 MILLISECOND DUR	Tested By ATION SHOCK	- Hearty,		
	Y Direction - Did	Any Bit Errors	Occur?		19
	Yes Address	Bit	:s	MAY 3 0 1975 (1) O Errors	
107 overnm	OROLA INC. ent Electronics Division	SIZE CODE IDENT A 94990		-P13721D	
	1201 F. McDOWELL ROAD 11 ISDALE, ARIZONA 85252	SCALE R	EVISION	SHEET 22	

AV.2.R. 10011_INIA. 2 LQ DWG FORMAT

			Tested by	Texton.	
			·	Limits	M 30
	Z Direct	ion - Did Any Bit	t Errors Occur?		" E
	No	• • • • • • • • • • • • • • • • • • •			
	Yes	Address	Bits	0 Errors	•
	X Direct	ion - Did Any Bit	t Errors Occur?		,
	No L-	en e			
	Yes	Address	Bits	0 Errors	
	12 MILLI	SECOND DURATION S	SHOCK	21 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 -	
	Y Direct	ion - Did Any Bit	t Errors Occur?		5
out!	No 1-				.
			Bits	0 Errors	
	169	Address	Dics	o Errors	
	Z Direct	ion - Did Any Bit	t Errors Occur?		
	No L	en e		ateuration (1944) ateurija direktaja direktaja dir	
			Dita	0 Errors	
	I GB	Address	Bits	O EFFOR	
	X Direct	tion - Did Any Bit	t Errors Occur?		
	No L				
				0 Errors	
	Yes	Address	Bits		
				01975	(1)
				ETELO E YAM	

MOTOROLA INC.	SIZE	CODE IDENT NO.	DWG NO.	, j	
Government Electronics Division	A	94990	12-P13721D		
8201 E, McDOWELL ROAD	22.11 5	<u> </u>	lou lou		
SCOTTSDALE, ARIZONA 85252	SCALE	REVIS	ION 21	IEET	23

	s/n	Date of Test	
7.4	CHASSIS ISOLATION Impedance 7		Limit ≥ 9 megohms
7.5	INPUT SIGNAL LOADING		
7.5.2	Current from INITIATE PULSE to G	nd <u>/.38</u> ma	≤ 2 ma
	Current from 2.4V to INITIATE PU	LSE <u>1.31 p</u> a	≥ 20 µa
7.5.3	Current from MEM SEL 1 to Gnd 1	.38 <u>I</u> na	≤ 2 ma
	Current from 2.4V to MEM SEL 1	.97 /ia	≤ 20 pa
7,5,4	Current from MEM SEL 2 to Gnd		≤ 2 ma
	Current from 2.4V to MEM SEL 2	1.38 ya	≥ 20 µ a
	Current from MEM SEL 3 to Gnd	<u>/.38</u> ma	≤ 2 ma
	Current from 2.4V to MEL SEL 3	134 ya	≤ 20 µ a
	Current from MEM SEL 4 to Gnd	1.38 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 4 _	.96 µa	≤ 20 µ a
7.5.5	Current from READ/WRITE to Gnd _	1002 ma	≤ 2 ma
	Current from 2.4V to READ/WRITE		≤20µa
7,5,6	Current from ADDRESS 20 to Gnd_	.99 ma	≤ 2 ma
	Current from 2.4V to ADDRESS 20_	634 pa	≤20 pa
	SIZE CODE IDENTIFY A PASSON A 94990	10. DWG NO.	21D

8201 E. MEDOWELL ROAD SCOTTSDALE, ARIZONA 65252

SCALE

REVISION

SHEET 24 s/n /04

Date of Test 6/6/75

	,						Limits
from	ADDRESS	21	to Gnd	,90	_ma		≤ 2 ma
from	2.4V to	AD	DRESS 21	5.93	-ya		≤ 20 pla
from	ADDRESS	22	to Gnd	<u>.97</u>	_ma		≤ 2 ma
from	2.4V to	AD	DRESS 2 ²	6.76	-pa		€ 20 µ a
from	ADDRESS	23	to Gnd	.90	_ma		≤ 2 ma
from	2.4V to	AD	DRESS 23	7.40			≤ 20 µ a
from	ADDRESS	24	to Gnd	.95	_ma		≤ 2 ma
from	2.4V to	AD	DRESS 24	7.8	3 ₄ a		≤20 µa
	from from from from from	from 2.4V to from ADDRESS from 2.4V to from ADDRESS from 2.4V to from ADDRESS	from 2.4V to AD from ADDRESS 2 ² from 2.4V to AD from ADDRESS 2 ³ from 2.4V to AD from ADDRESS 2 ⁴	from 2.4V to ADDRESS 2 ¹ from ADDRESS 2 ² to Gnd from 2.4V to ADDRESS 2 ² from ADDRESS 2 ³ to Gnd from 2.4V to ADDRESS 2 ³ from ADDRESS 2 ⁴ to Gnd	from 2.4V to ADDRESS 2 ¹ <u>5.93</u> from ADDRESS 2 ² to Gnd <u>.97</u> from 2.4V to ADDRESS 2 ² <u>6.76</u> from ADDRESS 2 ³ to Gnd <u>.90</u> from 2.4V to ADDRESS 2 ³ 7.40 from ADDRESS 2 ⁴ to Gnd <u>.95</u>	from ADDRESS 2 ¹ to Gnd	from 2.4V to ADDRESS 2^{1} <u>5 93 pa</u> from ADDRESS 2^{2} to Gnd <u>.97 ma</u> from 2.4V to ADDRESS 2^{2} <u>6 76 pa</u> from ADDRESS 2^{3} to Gnd <u>.90 ma</u> from 2.4V to ADDRESS 2^{3} <u>7.40 pa</u> from ADDRESS 2^{4} to Gnd <u>.95 ma</u>





MOTOROLA INO.	SIZE	CODE IDENT NO.	DWG NO.
Government Electronics Division	Α	94990	12-P13721D
8201 E. McDOWELL ROAD SCOTTSDALE, ARIZUNA 85252	SCALE	REVIS	ION SHEET 25

8/N	104	!					
Current	from	ADDRESS	2 ⁵	te			

Date of Test 6/6/25

Limits

To the second

C. Middle

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A STATE OF A

Current	from	ADDRESS	2 ⁵ to Gnd _	. 8 9	ma	≤ 2 ma
Current	from	2.4V to	ADDRESS 25	5.42	pa	€ 20 Na
			2 ⁶ to Gnd			∠ 2 ma
Current	from	2.4V to	ADDRESS 25_	5.52	μa ' n n n	a كز20 ك

* ** * * * * * * * * * * * * * * * * *		•	
Current	from ADDRESS	2 ⁷ to Gnd96 ma	≤ 2 ma
Current	from 2.4V to	ADDRESS 27 6.53 µa	1- 20/Va
Current	from ADDRESS	28 to Gnd ma	∠ 2 ma
Current	from 2.4V to	ADDRESS 28 / / / 0 pa	≤ 20 Na
Current	from ADDRESS	29 to Gnd 92 ma	∠ 2 ma
Current	from 2.4V to	ADDRESS 29 1.09 µa	عر 20 ≥ aلم 20 ≥
		2 ¹⁰ to Gnd . 77 ma	
Current	from 2.4V to	ADDRESS $2^{10} / 27 \mu a$	ك 2 ma الر20 ≟ 20 a
Current	from ADDRESS	2 ¹¹ to Gnd . 99 ma	≤ 2 ma
Current	from 2.4V to	ADDRESS 2 ¹¹ / 30 pa	= 20 pa
Current	from DATA IN	BIT 0 to Gnd 164 ma	<u> </u>
Current	from 2.4V to	DATA IN BIT 0 tot pa	~ 20 Na
		720	



MOTOROLA INC.
Government Electronics Division

SIZE

CODE IDENT NO. DWG NO. 94990

S/N 104

Tested By

	Limits
Current from DATA IN BIT 1 to Gnd 1.06 ma	≤ ? ma
Current from 2.4V to DATA IN BIT 1 7.32 pa	£ 20 pa
Current from DATA IN BIT 2 to Gnd	∠ 2 ma
Current from 2.4V to DATA IN BIT 2 6.71 pa	£ 20/2 a
Current from DATA IN BIT 3 to Gnd 1.03 ma	<u>≪</u> 2 ma
Current from 2.4V to DATA IN BIT 3 9.22 pa	≤ 20/2a
Current from DATA IN BIT 4 to Gnd / 02 ma	<u><</u> 2 ma
Current from 2.4V to DATA IN BIT 4 9.16 2	≤ 20/Ja
Current from DATA IN BIT 5 to Gnd 1.04 ma	∠ 2 ma
Current from 2.4V to DATA IN BIT 5 8.97 pa	a المر20 🛬
Current from DATA IN BIT 6 to Gnd 1.06 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 6 7.65	<_20, -a
Current from DATA IN BIT 7 to Gnd 104 ma	∠ 2 ma
Current from 2.4V to DATA IN BIT 7 7.31 pa	≤20/1'a
Current from DATA IN BIT 8 to Gnd / 03 ma	∠ 2 ma
Current from 2.4V to DATA IN BIT 8 7.73 µa	a سر 20
Current from DATA IN BIT 9 to Gnd .97 ma	<u>≤</u> 2 ma
Current from 2.4V to DATA IN BIT 9 8.09 µa	€ 20 µJa
보고 이번에 이번 모고 하는 다른 사람이 보고 하게 되는 다니라고 한 작가를 하셨다.	

WOTOBOLA INC.
Government Electronics Division

A

CODE IDENT NO. DWG NO.

12-P13**72**1D

SIZE

s/n /04

Date of Test 6/6/75

	Limits
Current from DATA IN BIT 10 to Gnd .98 ma	<u>∠</u> 2 ma
Current from 2.4V to DATA IN BIT 10 8.39 µa	£ 20/2
Current from DATA IN BIT 11 to Gnd 99 ma	€ 2 ma
Current from 2.4V to DATA IN BIT 11 8.09 pa	£ 20 p a
Current from DATA IN BIT 12 to Gnd /.04 ma	<u>∠</u> 2 ma
Current from 2.4V to DATA IN BIT 12 9.43 pa	∠20µa
Current from DATA IN BIT 13 to Gnd 1.04 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 14 9.12 pa	≤ 20/2a
Current from DATA IN BIT 14 to Gnd 1.05 ma	∠ 2 ma
Current from 2.4V to DATA IN BIT 14 8.93 / a	<u>در20</u> م
Current from DATA IN BIT 15 to Gnd / 06 ma	∠ 2 ma
Current from 2.4V to DATA IN BIT 15 609 12	€ 20µa
Current from DATA IN BIT 16 to Gnd / 03 ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 17 6.16 pa	€ 20 µa
Current from DATA IN BIT 17 to Gnd 105 ma	∠ 2 ma
Current from 2.4V to DATA IN BIT 17 7.24 va	€ 20 pa
마시얼마 하다 무슨 마음을 하는 것이 있었다. 그는 남은 사람들이 가는 것이 되었다고 있다고 있다.	



MOTOTOLA INC.
Government Electronics Division

SIZE

CCALE

CODE IDENT NO. DWG NO.

94990

Limit

7.6	VERIFICATION	OF OPEN	COLLECTOR	ON OUTPUT	SIGNALS	•
				•		

7.6.3	READ COMPLETE voltage	68	_ mv		∉ 100 mv
7,6,4	DATA OUT BIT 0 voltage	40	mv		≤ 100 mv
	DATA OUT BIT 1 voltage		mv	in a verification of the second of the seco	≤ 100 mv
	DATA OUT BIT 2 voltage	***************************************	mv		ತ 100 mv
	DATA OUT BIT 3 Voltage		mv		≤ 100 mv
	DATA OUT BIT 4 voltage		mv		≤ 100 mv
	DATA OUT BIT 5 voltage	20	mv		≤ 100 mv
	DATA OUT BIT 6 voltage	20	 mv	•	≤ 100 mv
	DATA OUT BIT 7 voltage	0	mv		≈ 100 my;
	DATA OUT BIT 8 voltage		mv		≤ 100 mv
	DATA OUT BIT 9 voltage	20	mv		≤ 100 mv
	DATA OUT BIT 10 voltag	e 20	mv		≤ 100 mv
	DATA OUT BIT 11 voltag		mv	•	≤ 100 mv
	DATA OUT BIT 12 voltag	e 20	mv		≤100 mv
	DATA OUT BIT 13 voltag	e 25	mv		: 100 mv
	DATA OUT BIT 14 voltag		mv		= 100 mv
	DATA OUT BIT 15 voltag		mv		≤100 mv
	DATA OUT BIT 16 voltag	*	— mv		<-100 mv
	DATA OUT BIT 17 voltag	**************************************	mv		≠ 100 mv
	and the control of th				





MOTOROLA	INC.
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→	s/n		Date of Test 6/6/75
		•	Tested By
		•	Limits
7.7	POWER CONSUMPTION (25°C)		HP 412 A
7.7.1	Memory +5V Voltage 5008	Volts	
	Memory -6.1V voltage6.016	Volts	
	45V Current 10.1	ma	
	+5V Power <u>50.U</u>	mw	
7.7.2	Memory -6.1V Current 3/	ma	
	Memory -6.1V Power 18.7	mw .	
7.7.3	Total Memory Idle Power 69.3	рw	170 mw max
7.7.5	Memory +5V Voltage 5.009	Volts	
	Memory -6.1V Voltage -4.109		
	+5V Current 650	ma	
	+5V Power <u>3255.9</u>	mw	
7.7.6	Momory -6.1V Current 220	ma	
	Mcmory -6.1V Power 1344.0	mw	
7.7.7	Total Active Power 4599.9	mW	7000 mw max.
7.8	READ COMPLETE TIMING		
7,8,5	Delay 390 ns		500 ns max.
	Duration 320 ns		250 ns min
			450 ns max.
			(M)
	ا معملاً أنا لما الأسكر مسارات الأراف	NT NO. DWG NO.	
overnmer	nt Electronics Division A 9499)U	12-P13721D

REVISION

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SHEET

8201 E. MCDOWELL ROAD COLLSDALF ARIZONA 85252

A IAOS

		•	•	<u>Limits</u>
8.7 &	READ CO	MPLETE/DATA OUTPUT	TIMING .	
3.8	DO-0	OKREJEC	T	en de la composition de la composition La composition de la
	DO-1	OK REJEC		
	DO-2	OK REJEC	T	
	DO-3	OKREJEC	T	
	DO-4	OKREJEC	et	
	DO-5	OK L REJEC	T	
	DO-6	OK V REJEC	T	
	DO-7	OKREJEC	CT	REFER TO TEST PRO
	DO-8	OKREJEC	T	
	DO-9	OKREJEC	CT	
	DO-10	OKREJEC	T	
	DO-11	OKREJEC		
	DO-12	OKREJEC		
	DO-13	OKREJEC	•	
	DO-14	OK V REJEC	•	
	DO-15	OKREJEC		
	DO-16 DO-17	OK REJEC		
	DO-11	OKREJEC		

CODE IDENT NO. DWG NO. SIZE Α

8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

SCALE

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SHEET 31

	s/n <u>/04</u>		Date of Test	6/7
			Lim	its
7.9	SYSTEM FUNCTIONAL TES			
7.9.2	Did an error occur?			•
	No X			
	Yes Address	Bits	0 e.	rrors
7.9.4	Did an error occur?			
	No X			
	Yes Address	Bits	0 e	rrors
7.9.10	Did an error occur?			
	No X			rrors
	Yes Address	DIUS		ITOES
7.9.16	Did an error occur?			
	ио <u>Т</u>			
•	Yes Address	Bits	, 0 °e	rrors
7.10	RANDOM ACCESS CAPABII	LITY		
			가는 기계하는데, 하루면도 가능한 이번 기계를 하는데, 그리고 하였다.	
7.10.8	Did an error occur?			
	Yos Address	Bits		rrors
7,10,7	Did an error occur?			
	Yes Address	R1ts		rrors
				(M)

AVICAN CLICK SCHLEN ANGE Government Electronics Division

SCOTTSUALE, AKIZONA 85252

94990

12-P13721D

SCALE.

REVISION

CHEET 32

	s/N 104	Dat	e of Test 6/6/7
		Tes	Limits
		•	
4	b) No X		
	Yes Address	Bits	0 errors
	c) No Y	*** **********************************	
	Yes Address	Bits	0 errors
.11	NON-VOLATILITY TEST		
11 7	Did an error occur?		
	Did the Circle Coods.		
6	No Y		
.11.9	No X Yes Address Bits		0 errors
.11.9	No X Yes Address Bits		0 errors
			0 errors
.12	Yes Address Bits		0 errors
,12 ,12,3	Yes Address Bits MEMORY SELECT TEST		
,12 ,12,3	Yes Address Bits MEMORY SELECT TEST Address (Octal)		0000
.12 .12.3	Yes Address Bits MEMORY SELECT TEST Address 0000 (Octal) Address 0001 0000 (Octal)		0000
.12 .12.3	MEMORY SELECT TEST Address 0000 (Octal) Address 0001 0000 (Octal) 0010 0000 (Octal)		0000
.12 .12.3	MEMORY SELECT TEST Address 0000 (Octal) Address 0001 0000 (Octal) 0010 0000 (Octal)		0000 0000 0000
.12 .12.3	Yes Address Bits MEMORY SELECT TEST Address 0000 (Octal) Address 0001 0000 (Octal) 0010 0000 (Octal) 0011 0000 (Octal) 0100 0000 (Octal)		0000 0000 0000 0000
.12 .12.3	Yes Address Bits MEMORY SELECT TEST Address 0000 (Octal) Address 0001 0000 (Octal) 0010 0000 (Octal) 0100 0000 (Octal) 0101 0000 (Octal)		0000 0000 0000 0000 0000
.12 .12.3	Yes Address Bits MEMORY SELECT TEST Address 0000 (Octal) Address 0001 0000 (Octal) 0010 0000 (Octal) 0101 0000 (Octal) 0110 0000 (Octal)		0000 0000 0000 0000 0000 0000
.12 .12.3	Yes Address Bits MEMORY SELECT TEST Address 0000 (Octal) Address 0001 0000 (Octal) 0010 0000 (Octal) 0101 0000 (Octal) 0110 0000 (Octal) 0111 0000 (Octal)		0000 0000 0000 0000 0000 0000





8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252	SCALE	l IREVIS	ION SHEET 33
Government Electronics Division	Α	94990	12-P13721D
MOTOROLA INC.	SIZE	CODE IDENT NO.	DWG NO.

t.	•				1		* .
	8/N	104		• • • • • • • • • • • • • • • • • • •	Dato of Tes		S Commencery
T			· · · · · ·		lested by	Limits	The state of the s
	Address	1011 0000	(Octal)			0000	
		1100 000	O (Octal)			0000	
		1101 0000	(Octal)			0000	5 1
		1110 0000	Octal)			0000	
7.12.6	Did an	error occur	?				
	No X						<i>5</i> *3
	Yos	Address	Bits			0 errors	3
7.13	WORST C	ASE PATTERN	TEST				
7.13.2	Did an	error occur	?				
	No X	en de la companya de ■ Transportation de la companya de					Ĵ
	Yes	Address	Bits			0 error	
7.13.3	. Did an	error occur	?				
	№ Д						
	Yes	Address	Bit	S		0 error	B (4)
							**
							A Transmitter
						6	
							1
Moro	MOLA	INC. SI	ZE CODE IDEN				I
Governmen			1 94991	n I	12-01372	1 n	L.J

REVISION

SCALE

SHEET

34

8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

	s/n _	104			Date of Te	st <u>6/6/75</u>
7.13.4		Did an er:	ror occur?			Limits
			Address	Bit		0 errors
	3	٠٥ <u>ــــــــــــــــــــــــــــــــــــ</u>	ror occur?			
		les	Address	Bit		0 errors





Government Electronics Division

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SIZE

CODE IDENT NO. DWG NO.

94990

12-P13721D

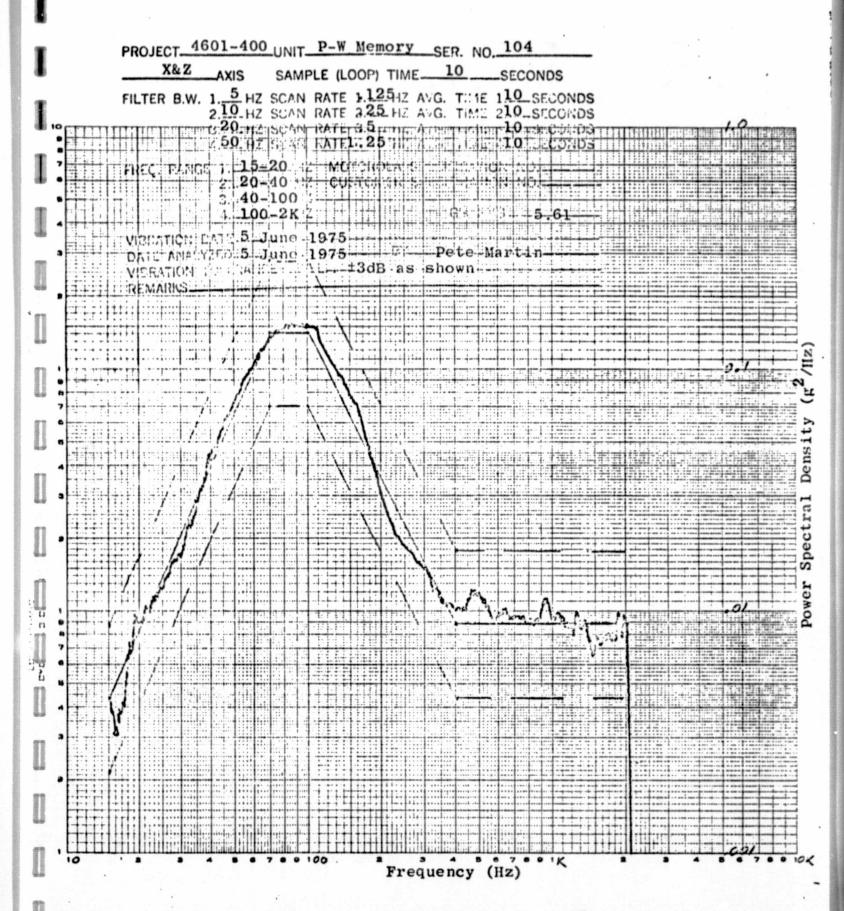
8201 E. MCDOWELL ROAD SCOTTSDALE, ARIZONA 85252

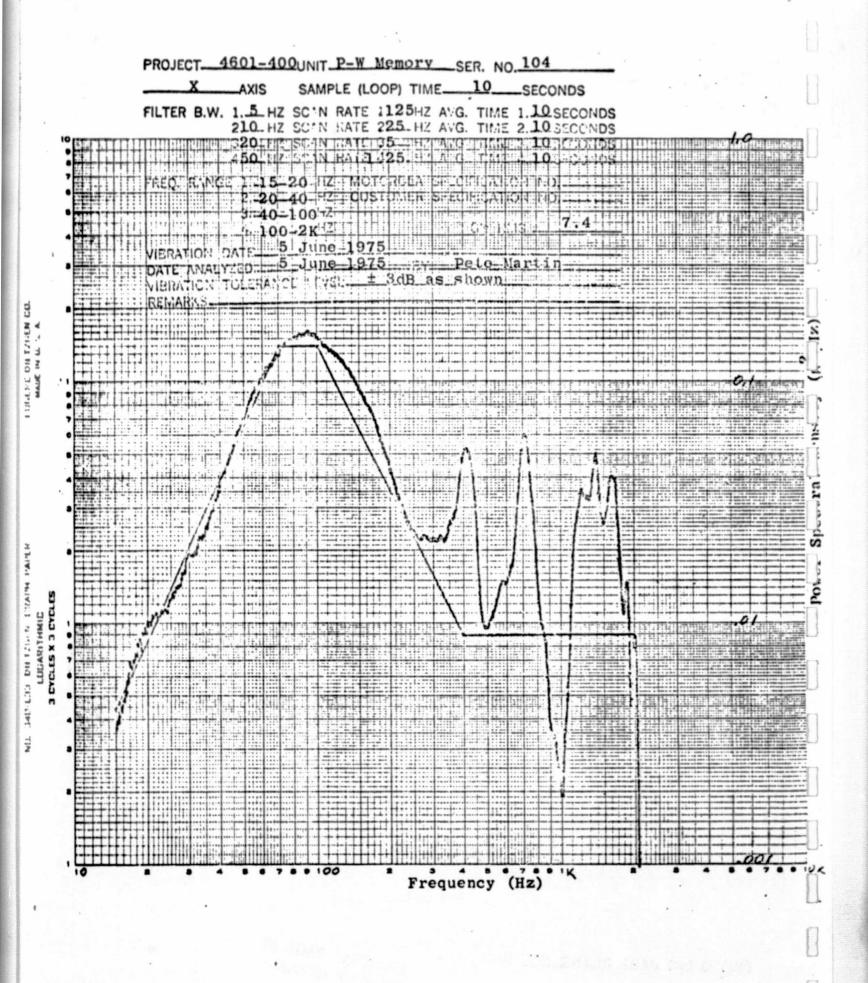
SCALE

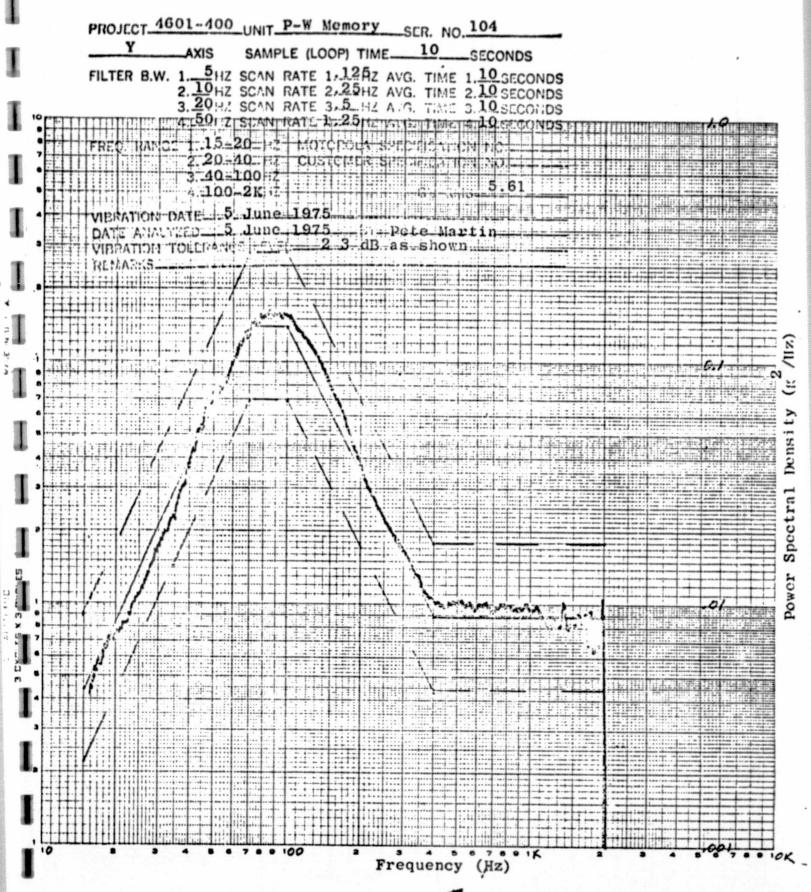
A

REVISION

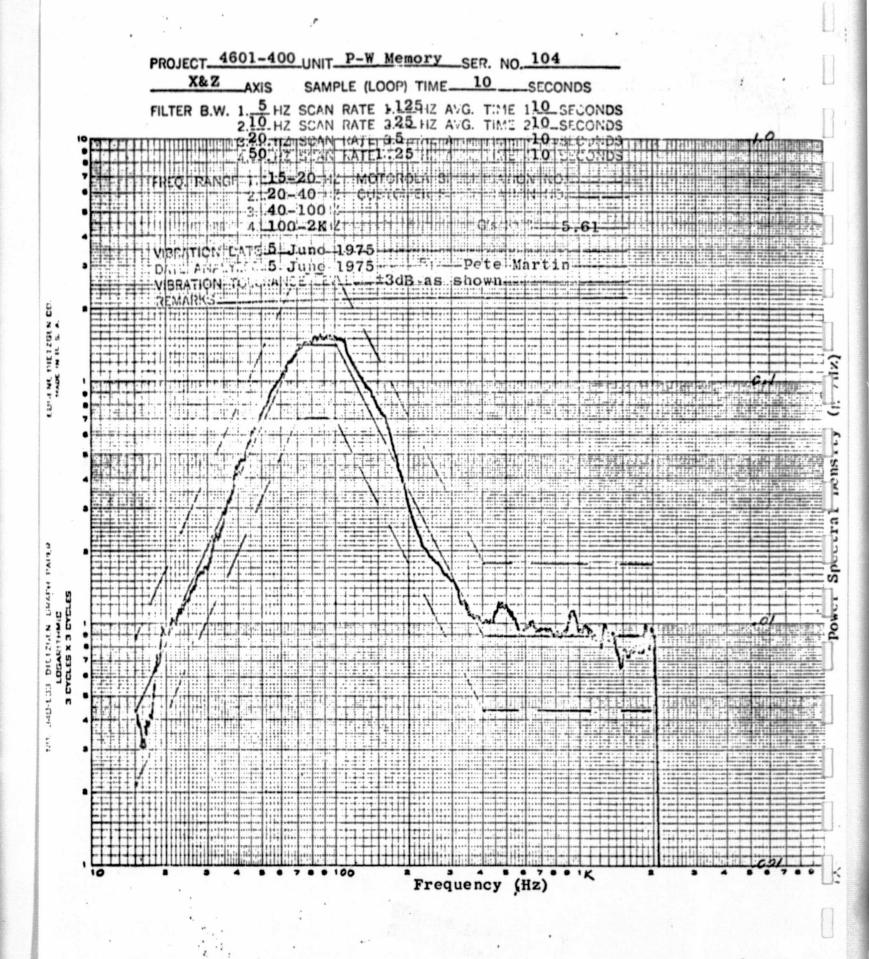
SHEET 35







ORIGINAL PAGE IS



PROJECT_4601-400 UNIT_P-W Memory_SER. NO. 104 SAMPLE (LOOP) TIME 10 ___SECONDS FILTER B.W. 1._5 HZ SCAN DATE 1._126 AVG. TIME 110_SECONDS 2.10 HZ SC'N RATE 2._25HZ AVG. TIME 210 SECONDS 3.20 MZ SCAN RATE 3. 5.HZ AVG. THIS 310 SECONDS 1,50,112 | CATE 1,25 | A G | G | G | CATE | 3_40-100 ...100-2K MB(ATICN DAT: 5-June-1975-DATE AND TO STANCE IN THE NAME OF THE PROPERTY REPARCE Response of top cover Frequency (Hz)

POOR QUALITY

MOTOROLA INO.	VIBRATION TEST	, y
8HEETOF	DATE 5 June 75	
	UNIT Printed Wire Menong	
CONTROL NO. OF 902 OPERATOR Set 110		2 / 2
ARCERVED LA MAN	. I dan	

CYCLE TIME 4.5 AIN FREQ. 5 TO 2000 Hz

SPEC DETAILS

AXIS RUN NO.	TIME	TIME STOP	ACCOM: SCATED VIB. TIME	UNIT SER. NO.	DISPLACEMENT INCHES D.A.	ACCELERATION X RMS X PK G'S MV (RMS)	REMARKS -
7	12:44	13:46	2412	104	NA	5.6100	shapedrandom.
2:			4.3MIN	104	.33	1045 70431	Sime sweep 5-110-24HZ
1	13:20	13:25	4.3MIN	104	.33	1045	ine sweep 5-110-2KHZ
<u>``</u>	13127	13:29	ZMIN	104	NA	5.6100	shaped random.
Y	141.45	14:47	ZMIN	104	NA	5.61 rm 56	shaped random
Y	14:48	14:53	4.3 MIN	104	. 33	10+5	sine sweep 5-110-2KHE
					·		
				'			
				·			

Project

Field - 400

Specification

12 - P 13 750

Operator

Observer

LEE ISULDIN Dale 2 25 Model N/A W.O. 3039 CONTROL V./
HIGH VACUUM TEST Serial Vacuum System No. PRESSURE REMARKS TIME (mm Hg A) TART TO HI VAC 010 6.3 X10 1000 2×10-5 1030 1.4110-5 1100 1.1x10-5 15 4.4 XIC-6 END TEST 130 49116-6

ALAMAN MAISS MAD

Page / of

(M)	MOTOROLA Severament Bleetrenies	INO.
~~~	14-11	

# SHOCK TEST (DROP)

PROJECT 4/01-400  DATE 5-30-75	TYPE OF TEST	A	
SHEET/_OF/	☐ FREE FALL DROP		
W.O. NO. 3040			
CONTROL NO. //	B		
unit			
SERIAL NO			
OPERATOR Year M	c/ []		
OBSERVER Lec Go Kolon	la constanta de		
VIBRATION MOUNTS None			
NO. OF DROPS PER FACETO	TAL NO. OF DROPS 6		
ACCELERATION 30 G'S			•
PULSE DURATION 65/12	AS		
SPEC DETAILS /2 - 0/3722 /			4

PROGRAMMER PRESSURE		PAD AND P	LATE CONFIGURATION	2
TYPE OF WAVESHAPE Jackaine	ITEM No.	PART NO.	DESCRIPTION	
BANDPASS FILTER LOW FR. Hz	1	11186 2359	alum plate	187
3700 HIGH FR. Hz	2	11072796	1"red open	(B)
REMARKS 3 dages of 6 ms & 3 dages at 12 ms	3	11/ 2358	a lum plate	17
	4			
Pala for 12 as; 1-8xxx plantic	5			) in the second
2-8x814 melolin	6			
3-8x8xt nulthin	7			ि इन्
3-1 Han closed	8			
1-1" lile open	9			
lons	/1	LMS		ji

		(://4)										1 5 777	<u> </u>								
AXIS	FACE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
	1	1										1									-
	2																				
	1	1										1									
	2	1																			
	1	1	ş									1									
C	3		•																		
																					20.3

test complete.

;**,** 

1.3233 4/74 CTL 734

#### ATTACHMENT IV

ACCEPTANCE TEST DATA SHEET
LOW POWER RANDOM ACCESS
SPACECRAFT MEMORY
PART NO. 12-P13721D
SERIAL NUMBER 105
(35 PAGES)

*APPLICA	TION							RI	EVIS	310!	18								130901-010	•	
SXT ASSEMBLY	USED	NC	1.1	1			·Đ	ESCRI	PTIC	N					DAT	ΤE		A	PPR	OVE	<u>D</u>
			_] x:	ı	Ini	tial	. Re	eleas	e									_		<del>~</del>	
			_ x	2				ted o		ige	s pr	ior		3	- 16	:-7	3	4.	4	•••	2.
			X	<u>3</u>				.9V 1	_	-6.	LV			6-	·18·	<u>-7</u>	3_	1/.	Je.	ee z	<u> </u>
ASTERISK INDICATES DA WHICH IS NORMANDATO - FOR INFORMATION ON	RY		X4		pag Cha	ges ange	10, we	00mw 17, ight	19 fr	, 3 om	0. 6.0			7-	-24	/-;	73	11.	J.	rre	امنا
			XS					t 5. cha					5.	5	- 10	•	75.	1	ر ويلا	2	()
***************************************			X	5	Rev	ise	d po	er M	00	57	345			4	-28	₹•=	75	~	£.	دبر باساد	الر
			•			4	١.	10	ا د ر	5		•									
						ん		10	2	5											
						·人		10	<b>)</b> [												
CHARLES THE THE THE				<del></del>		T		10	) [[]	<b>5</b>											
HEET 27 28 2	9 30 31	323	3 34	35		·人 —															
HEET \$7 28 2 EV STATUS REV	9 30 31 x 5 x5	32 3 X1 3	3 34 (1 X1	35	X1 X			x1 X	X1	  X1	_		_	7		7-					_
RV STATUS REV SHEETS SHEET	9 30 31 x 5 x5 1 2	32 3 X1 3	3 34	35	X1 X	1 X1 3 9			X1	  X1	_	(6 X)	_	7		7-					_
RV STATUS REV P SHEETS SHEET OR ASSOCIATED LISTS	9 30 31 x 5 x5 1 2 SEE	32 3 X1 X 3	33 34 (1 X1 4 5	35 X1 6	X1 X	3 9	10	X1 X1 11 12	X1	  X1	_		_	7		7-					_
EV STATUS REV PSHEETS SHEET  OR ASSOCIATED LISTS WEERPRET DRAWING IN	9 30 31 x 5 x5 1 2 SEE ACCORDAN	32 3 X1 X 3	33 34 31 X1 4 5 TH STA	35 X1 6	X1 X 7 8	3 9	10	X1 X1 11 12	X1	  X1	_		_	7		7-					_
REV STATUS REV SHEETS SHEET  OF SHEETS SHEET  OR ASSOCIATED LISTS  WERPRET DRAWING IN INCESS OTHERWISE SPECIALL DIMENSIONS ARE INCHES AND END USE.	9 30 31  K 5 X5  1 2  SEE  ACCORDAN  IN CHAP  FOR CHAP	32 3 X1 2 3 CE WI'	33 34 (1 X1 4 5	35 X1 6	X1 X 7 {	SCRIE	ED B	X1 X1 11 12		X1 14	15 I	6 17 /N	18 C.	/82	20 01 E	21 AS	L 22	2 23 DOW		25 ROA	10
REV STATUS REV REV SHEETS SHEET REPRET DRAWING IN RESS OTHERWISE SPECIALL DIMENSIONS ARE INCHES AND ENDUSE. TOLERANCES SEE NO	9 30 31  x 5 x5  1 2  SEE  ACCORDAN  IN CHAPTE	32 3 X1 2 3 CE WI BY 1	33 34 (1 X1 4 5 TH STA	35 X1 6 WDAF Wee	X1 X 7 { CDS PRI d	SCRIE	ED B	X1 X1 11 11 12 Y		X1 14	15 I	6 17 /N	18 C.	/82	20 01 E	21 AS	L 22	2 23 DOW	24 ELL	25 ROA	10
REV STATUS REV  OF SHEETS SHEET  OR ASSOCIATED LISTS  NTERPRET DRAWING IN  NLESS OTHERWISE SPECIALL DIMENSIONS ARE  INCHES AND END USE.	9 30 31  x 5 x5  1 2  SEE  ACCORDAN  IN CHA FOR CHA TE MFO	32 3 X1 3 CE WI' BY I R N	33 34 31 X1 4 5 TH STA	35 X1 6 WDAR Wee	X1 X 7 { CDS PRI d 46 163	SCRIE	ED B	X1 X3 11 12 Y	X1 X1 2 13	X1 14 Po	LA ronics	IN Divis	C.	/82 SC DATE	20 01 E OTT	AS SI	T Mc	DOW , AR	ELL IZON	25 ROA A 85	10 525
REV STATUS REV P SHEETS SHEET  OR ASSOCIATED LISTS  VTERPRET DRAWING IN NUESS OTHERWISE SPECIALL DIMENSIONS ARE INCHES AND END USE. TOLERANCES SEE NO	9 30 31  x 5 x5  1 2  SEE  ACCORDAN  IN CHA  FOR CHA  TE MFC  CON  NO.  REL  NO.  APF	32 3 X1 3 CE WITE BY 1 CE WITE	33 34 (1 X1 4 5 TH STA H. T	35 X1 6 Wee	X1 X 7 8 05 PRE d 163 576	SCRIE	ED B	X1 X1 X1	X1 2 13 ACC: LOW CRA:	X1 14 PO FIECT PO FT	ANCI WER MEMONT N	/N: Divis	C. Sion /	/82 SO DATI AC	20 01 E OTT	AS' SD	T Mc	DOW , AR PAC-P1	ELL IZON E-370	25 ROA A 85	10 525



SCOPE

This test data sheet is to be used to record data as required by the Acceptance Test Procedure for the Low Power Random Access Spacecraft Memory.

- 2. REFERENCE INFORMATION
- .2.1 SPECIFICATIONS APPLICABLE

8-562-P-24

Low Power Random Access Spacecraft

Memory

12-P13722D

Acceptance Test Procedure, Low Power Random Access Spacecraft Memory

3. TEST DATA

Unit S/N 105 Start Date of Tests 5/15/73

Tested by

## ATP PARA. NO.

3.1 EQUIVALENT TEST EQUIPMENT

DC N. 11 1 1 1 1 1 2 8 A C-1 A

DIG.TAL VOLTMETER FLUKE BIZOA (MULTIMETER)

COUNTER HT 5245 L

4. PHYSICAL CHARACTERISTICS

Limit

6.1 WEIGHT

Weight of LP-RASM - 5.594

6.5 pounds (aluminum)

5.8 pounds (magnesium)

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**Pounds** 

SHEET

Date of Test · Tested By _

6.2 **DIMENSIONS** 

Limit

Access to the second se

inches

inches

inches

inches

.630 inches

-  $H \times W \times D = 158.5$  inches

≤ 160 inches

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AUS B. 1004 1004 2/CO DWC CODIAT

S/N_	105	Date of Test 5/15/75
and the second s	* * * * * * * * * * * * * * * * * * *	Tosted By Control

7.4	CHASSIS ISOLATION	Limit
	Impedance >9meg	≥ 9 megohm
7,5	INPUT SIGNAL LOADING	
7.5.2	Current from INITIATE PULSE to Gnd /109 ma	≤ 2 ma
	Current from 2.4V to INITIATE PULSE	≥ 20 µa
7.5.3	Current from MEM SEL 1 to Gnd /. 105 ma	., <b>≤</b> 2 ma
	Current from 2.4V to MEM SEL 1	≥ 20 µ a.
7.5.4	Current from MEM SEL 2 to Gnd / 109 ma	≤ 2 ma
<u>.</u>	Current from 2.4V to MEM SEL 2 . 62 ya	≤ 20 µa
	Current from MEM SEL 3 to Gnd 1.109 ma	r ≤ 2 ma
	Current from 2.4V to MEL SEL 3 82 ya	≤ 20 µ a
	Current from MEM SEL 4 to Gnd 1.105 ma	<b>≤ 2 ma</b>
	Current from 2.4V to MEN SEL 4	≤ 20 µ a
7.5.5	Current from READ/WRITE to Gndma	≤ 2 ma
	Current from 2.4V to READ/WRITE 1.54 ya	≥20 Na
7.5.6	Current from ADDRESS 20 to Gnd	≤ 2 ma
	Current from 2.4V to ADDRESS 20_5.78 pa	. ≤20 ya

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8/N 105



Date of Test 5/15/75
Tested By

	Limits
Current from ADDRESS 2 to Gnd 942ma	<b>≤</b> 2 ma
Current from 2.4V to ADDRESS 21 5.33 pa	. ≤ 20 Ha
Current from ADDRESS 22 to Gnd /.0/7 ma	<b>≤</b> 2 ma
Current from 2.4V to ADDRESS 22 6.35 pa	€ 20 µ a
Current from ADDRESS 23 to Gnd 940 ma	., <b>£ 2</b> ma
Current from 2.4V to ADDRESS 236,74 µa	≤ 20 _µ a
Current from ADDRESS 24 to Gnd 994 ma	<b>\$ 2</b> ma
Current from 2.4V to ADDRESS 24 7.5/ a	\$ 20 µa

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8/N 105



Date of Test 5/15/75
Tested By

	2 ⁵ to Gnd 943 ma ADDRESS 2 ⁵ 6.02 µ2	<u>Limits</u> <u>≤</u> 2 ma <u>≤</u> 20 μa
	2 ⁶ to Gnd .931 ma ADDRESS 2 ⁵ 5.7/ wa	کے 2 ma کے 20 ع

			1 ·	
				<b>≤</b> 2 ma
Current	from	2.4V to	ADDRESS 27 6.68 µa	4 20/Ja
Current	from	ADDRESS	28 to Gnd / 039 ma	€ 2 ==
				ع 20 ہے
Current	from	ADDRESS	29 to Gnd / 0/6 ma	∠ '2 ma
				عر 20 کے
Current	from	ADDRESS	2 ¹⁰ to Gnd 9/0 ma	<u>∠</u> 2 ma
				ع لر 20 کے
Current	from	ADDRESS	2 ¹¹ to Gnd , 905 ma	≤ 2 ma
				= 20 µ2
Current	from	DATA IN	BIT 0 to Gnd 1.045 ma	<u> </u>
				<u>د</u> 20 مر
	Current Current Current Current Current Current Current Current Current	Current from	Current from 2.4V to  Current from ADDRESS  Current from ADDRESS  Current from 2.4V to  Current from ADDRESS  Current from ADDRESS  Current from 2.4V to  Current from 2.4V to  Current from ADDRESS  Current from ADDRESS  Current from DATA IN	Current from ADDRESS 27 to Gnd / .005 ma  Current from 2.4V to ADDRESS 27 6.68 µa  Current from ADDRESS 28 to Gnd / .039 ma  Current from 2.4V to ADDRESS 28 / .56 µa  Current from ADDRESS 29 to Gnd / .06 ma  Current from 2.4V to ADDRESS 29 / .67 µa  Current from ADDRESS 210 to Gnd 9/0 ma  Current from 2.4V to ADDRESS 210 / .59 µa  Current from ADDRESS 211 to Gnd .905 ma  Current from 2.4V to ADDRESS 211 / .60 µa  Current from 2.4V to ADDRESS 211 / .60 µa  Current from DATA IN BIT 0 to Gnd / .045 ma  Current from 2.4V to DATA IN BIT 0 7 46 µa

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# Date of Tost Tested By

	Limits
Current from DATA IN BIT 1 to Gnd /.037 ma	<b>≤</b> 2 ma
Current from 2.4V to DATA IN BIT 1 6.85 pa	عدر 20 کے
Current from DATA IN BIT 2 to Gnd 1.052 ma	<b>∠</b> 2 ma
Current from 2.4V to DATA IN BIT 2 2.09 pa	£ 20/2 a
Current from DATA IN BIT 3 to Gnd 1.029 ma	<b>≤</b> 2 ma
Current from 2.4V to DATA IN BIT 3 8.20 pa	∠ 20/2a
Current from DATA IN BIT 4 to Gnd / O// ma	∠ 2 ma
Current from 2.4V to DATA IN BIT 4 7.20 Na	< 20 Na
Current from DATA IN BIT 5 to Gnd /048 ma	<b>∠</b> 2 ma
Current from 2.4V to DATA IN BIT 5 7.45 va	عدر20 ك
Current from DATA IN BIT 6 to Gnd /016 ma	<b>∠</b> °2 ma
Current from 2.4V to DATA IN BIT 6 5,48 2	∠20,√a
Current from DATA IN BIT 7 to Gnd 0.992 ma	∠ 2 ma
Current from 2.4V to DATA IN BIT 7 5.5/ pa	≤ 20µ2
	<u></u> ∠ 2 ma
Current from DATA IN BIT 8 to Gnd 0.996 ma  Current from 2.4V to DATA IN BIT 8 5.83 Ma	= 2 ma <u>₹</u> 20 μ a
Current from DATA IN BIT 9 to Gnd 0.970 ma	∠ 2 ma
Current from 2.4V to DATA IN BIT 9 6.00 pa	< 20 pm

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		:		•	Limits
				BIT 10 to Gnd 0.97/ ma  DATA IN BIT 10 6.01 pa	£ 2 ma £ 20µa
•					∠ 2 ma
				DATA IN BIT 11 6.04 Na	20 ma
				BIT 12 to Gnd <u>0.990</u> ma	∠ 2 ma
Current	from	2.4V	to	DATA IN BIT 12 560 µ 8	
				BIT 13 to Gnd <u>0.99/</u> ma	≤ 2 ma
				DATA IN BIT 14 5,64 µa	<u>∠</u> 20µa
				DATA IN BIT 14 5.36 NR	ے 2 ma 20 سے 20
				BIT 15 to Gnd <u>0884</u> ma	≤ 2 ma
				DATA IN BIT 15 4, 17 µa	≥ 20, Na
Current	from	DATA	IN	BIT 16 to Gnd <u>874</u> ma	€ 2 ma
Current	from	2.4V	to	DATA IN BIT 17 4.66 µa	≥ 20 µa
				BIT 17 to Gnd 0.879 ma	<b>∠</b> 2 ma
current	ITOM	2.47	το	DATA IN BIT 17 4,77 va	عر20 کے

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Limit

7.6	VERIFICATION OF OPEN COLLECTOR OF	ON OUTPUT SIGNALS
7,6.3	READ COMPLETE voltage 20.0	_ mv ≤ 100 mv
7.6.4	DATA OUT BIT 0 voltage /0.0	mv 100 mv
	DATA OUT BIT 1 voltage /O.O	mv ≤ 100 mv
	DATA OUT BIT 2 voltage 5.0	mv
	DATA OUT BIT 3 voltage /O.O	mv <b>\$ 1</b> 00 mv
	DATA OUT BIT 4 voltage 5.0	_ mv / ≤ 100 mv
	DATA OUT BIT 5 voltage	mv ≤ 100 mv
•	DATA OUT BIT 6 voltage O.O	mv ′ ≤ 100 mv
	DATA OUT BIT 7 voltage O.O	mv
	DATA OUT BIT 8 voltage 10.0	mv ≤ 100 mv
	DATA OUT BIT 9 voltage 30.0	mv <b>≤ 100</b> mv
	DATA OUT BIT 10 voltage /5.0	mv 100 · mv
	DATA OUT BIT 11 voltage 30.0	mv ≤ 100 mv
	DATA OUT BIT 12 voltage 20.0	mv ≤ 100 mv
	DATA OUT BIT 13 voltage 20.0	mv
	DATA OUT BIT 14 voltage 205	mv
	DATA OUT BIT 15 voltage /5,0	mv ≤ 100 mv
	DATA OUT BIT 16 voltage 35.0	<u>)</u> mv <b>≤100</b> mv
	DATA OUT BIT 17 voltage 25.0	O mv ≤ 100 mv

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Tested By



Limits

7.7 POWER CONSUMPTION (25°C)

7.7.1 Memory +5V Voltage +5.001 Volts
Memory -6.1V voltage -6,/03 Volts

+5V Power 52.5

Memory -6.1V Power 20.2

7.7.2 Memory -6.1V Current 3.3 ma

7.7.3 Total Memory Idle Power 72.7 mw

170 mw max

7.7.5 Memory +5V Voltage <u>+5.006</u> Volts

Memory -6.1V Voltage -6./05 Volts

+5V Current

280 ma

+5V Power

3404 mw

7.7.6 Memory -6.1V Current <u>220</u> ma

Memory -6.1V Power 1343 mw

7.7.7 Total Active Power 4747 mw

7000 mw max.

7.8 READ COMPLETE TIMING

7.8.5 Delay <u>380</u> ns

Duration 370_ ns

500 ns max. 250 ns min

450 ns max.

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8/	N <u>105</u>	<del></del>	•	Date of Test	5/15/75.
	•	•	•	Tested by _	C. J. Gandele!
.8.7	READ CO	MPLETE/DATA	. ' A OUTPUT TIM	ING	LIMITS
.8.8	<b>DO-O</b>	ok	REJECT_	•	
	DO-1	OK	REJECT_		
•	DO-2	OK	REJECT		
	DO-3	ok	REJECT		
	DO-4	OR ~	REJECT	<del></del>	
	DO-5	OK 🗸	REJECT	*	
	DO-6	OK 🗸	REJECT		•
	DO-7	OK V	REJECT		REFER TO
	DO-8	OK	REJECT	•	TEST PROC.
	DO-9	or	REJECT		
	DO-10	OK	REJECT	e es	
•	DO-11	OK	REJECT	: +	
	DO-12	ок <u> </u>	REJECT	<del>-</del>	
- • • • • • • • • • • • • • • • • • • •	DO-13	or	REJECT	. i	
	DO-14	OK	REJECT		
	DO-15	OK	REJECT		
	DO-16	OK	REJECT		
	DO-17	OK	REJECT		

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SIZE A CODE IDENT NO. DWG NO.

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•:			•	•		
	8/N <u>(05</u>	•			Date of Tes Tested By	5/15/75 52 Emilia
219 1	•					Limits
7.9	SYSTEM FUNCTIONAL	L TEST				
7.9.2	Did an error occi	ır?			•	
	Yes Address	· ·	Bits			0 errors
7.9.4	Did an error occu	ur?				
	Yes Address		Bits	•	; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ; ;	0 errors
7.9.10	Did an error occu	ur?	•			
	Yes Address		Bits			0 errors
7.9.16	Did an error occi	ur?				
•	Yes Address	·.	Bits	•		0 errors
7.10	RANDOM ACCESS CA	PABIL	I <b>TY</b>			
7.10.6	Did an error occ	ur?				
	Yes Addres	8	Bits			0 errors
7.10.7	Did an error occ	ur?				
	Yes Addr	ess _	Bits _			.0 errors
	POLA INC. t Electronics Division	SIZE A	CODE IDENT NO. 94990	DWG NO.	12-P13	721D
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	8/N 105	Da ·	te of Test <u>5/15/55</u>
			sted By
			Limits
	b) No		
	b) No Address	Bits	0 errors
	c) No		
	Yes Address	Bits	0 errors
.11	NON-VOLATILITY TEST		
.11.7	Did an error occur?		
.11.9	No	en de la companya de La companya de la co	
	Yes Address Bits		0 errors
1.12	MEMORY SELECT TEST		
.12.3	Address Oppo (Octal)		0000
.12.4	Address 0001 Octal)		0000
	0010 0000 (Octal)		9000
	0011 (Octal)		0000
	0100 <u>000</u> (Octal)		0000
	0101 <u>000</u> 0 (Octal)		0000
	0110 0000 (Octal)		0000
	0111 0000 (Octal)		0000
	1000 <u>0000</u> (Octal)		0000
	1 1001 0000 (Octal)		0000
	1010 (Octal)		<b>°0000</b>

MOTOROLA INC.
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SIZE

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CODE IDENT NO. DWG NO.

	8/N 105			est 5/15/75
	•	T	ested By	Se Leanleh
			•	Limits
	Address 1011 0000 (Octal)			0000
	1100 0000 (Octal)		rain kanalasi Kanalasi	0000
	1101 0000 (Octal)	•		0000
	1110 <u>CCC</u> C(Octal)		•	0000
7.12.6	Did an error occur?			
	No			
	Yes Address Bits			0 errors
7.13	WORST CASE PATTERN TEST			
7.13.2	Did an error occur?			
	Yes Address Bits			0 errors
7.13.3	Did an error occur?			
	Yes Address Bits			0 errors

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	•		. :	•	•	•
<b>8/</b> N	1 105	•	· (:		of Test	
	•		V		Lim	. 1
7.13.4 a)	Did an error	occur?				
	Yes Ad	ldress	Bit	•	0 е	rrors
<b>b)</b>	Did an error	occur?				
	No Ad	idragg	P4+		0 e	rrors
	***************************************					•
			1			
MOTORO	DLA INC.	1	IDENT NO. DW	G NO.		
Government Elec	tronics Division	A 94	1990 c	C	<b>12-</b> P13721D	(M)
SCOTTSDALE,	OWELL ROAD ARIZONA 85252	SCALE	REVISION		SHEET	5

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s/	N	105	
	-		

DATE OF TEST & TESTED BY

<b>!</b>	TEMPERATURE TEST	•		•			LIMITS
1.2.1	TIME 6:30	V (4) (1) (1) (1) (2)					
3.2.2	LOW TEMPERATURE				•		
	THERMISTOR RESIS	TANCE				•	
•	150 MINUTES 22	1,2 K	OHMS				
	160 MINUTES 22	1,5 K	OHMS	% CHANGE	· · · · · · · · · · · · · · · · · · ·		
	170 MINUTES	к	OHMS	% CHANGE	•		
**************************************	189 MINUTES	к	OHMS	% CHANGE		•	ingera ( • 1.50) ••••••••••••••••••••••••••••••••••••
	190 MINUTES	к	OHMS	% CHANGE			
.2.3	DID AN ERROR OCC	cur?					
	NO X						•
	YES ADI	RESS	:	BITS			O ERRORS
		, <del>- 1</del> 101	LTS.	+5 V	VOLTAGE	6,255	VOLTS
.2.4	-6.1 V VOLTAGE -	<u>405</u> VU					
.2.4	-6.1 V VOLTAGE				CURRENT		
.2.4		1 <u>2.8</u> ma		+5 V	CURRENT POWER	10.3	ma
.2.4	-6.1 V CURRENT -	12.8 ma 81,99 mw		+5 V +5 V		10.3	ma
	-6.1 V CURRENT - -6.1 V POWER	12.8 ma 81.99 mw LE POWER	136,12	+5 V +5 V	POWER	/0, 3 54.13	ma mw 170 mw MAX
	-6.1 V CURRENT6.1 V POWER  TOTAL MEMORY IDI -6.1 V VOLTAGE -	12.8 ma 81,99 mw LE POWER 6.401 VO	<u>1<b>36.</b>12</u> LTS	+5 V +5 V mw	POWER	10, 3 54.13 5,250	ma mw 170 mw MAX VOLTS
	-6.1 V CURRENT6.1 V POWER TOTAL MEMORY IDI	12.8 ma 81.99 mw LE POWER 6.401 VOI	136,12 LTS 240	+5 V +5 V mw +5 V +5 V	POWER	5,250 660	ma mw  170 mw MAX  VOLTS ma 670

8701 EAST McDOWELL ROAD SCOTTSDALE, ARIZONA 85257

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SCALE REVISION

S/N	105		DATE O	F TEST 5/20/75
		•	TESTED	BY Forlal
	•		•	
610	<b>G</b>	•		LIMITS
8,2.6	DID AN ERI	ROR OCCUR?		
	NO X		•	
	YES	ADDRESS	BIT	O ERRORS
8,2,8	WC a) DII	O AN ERROR OCCUR?		
	NO X			
	YES	ADDRESS	BIT	0 ERRORS
	WC b) DID	AN ERROR OCCUR?		
	NO X			
	YES	ADDRESS	BIT	0 ERRORS
		AN ERROR OCCUR?		
	NO X			
	YES	ADDRESS	BIT	0 ERRORS
		AN ERROR OCCUR?		
	NO X YES	ADDRESS	BIT	O ERRORS
	100	· ADDIMOS		OBRORS
8.2.11	. WC a) DID	AN ERROR OCCUR?		
	ио 🗶			
	YES	ADDRESS	BIT	O ERRORS
	ROLA II	V Co.	NO. DWG NO.	

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8201 EAST MEDOWELL ROAD					
SCOTTSDALE, ARIZONA 85257	SCALE		REVISION		SHEET

			• •	• .		
s/N	105			· •	DATE OF TEST	5/20 75
					TESTED BY	Pell:
•		•		•		
	•				•	<u>LIMITS</u>
8.2.11	(Cont.)			• •		
	WC b) DID AN	ERROR OC	CCUR?	•		
	NO X					
	YES	ADDRESS	3	BIT	•	O ERRORS
	WC c) DID AN	ERROR O	CCURY		Qi	
	NO X		en e			
	YES	ADDRESS	S	BIT		O ERRORS
	WC d) DID AN	ERROR O	CCUR?			
	NO U, DID III		,		•	
		ADDRES	220	D T M		O Ennong
	YES X	ADDRES	s <u>300(</u>	. D11		O ERRORS
8.3	INTERMEDIATE	TEMPERA	TURE TEST			
	TIME 10:45		<b>,</b>	. •		
				•		
8.3.2	TIME THE	RMISTOR	READING.	DID ANY	ERROR OCCUR?	
	10:55	128	K OHMS	NO X	YES	O ERRORS
			K OHMS	NO NO	YES	O ERRORS O ERRORS
			K OHMS	NO	YES YES	O ERRORS O ERRORS
			K OHMS	NO	YES	O ERRORS
			K OHMS	NO	YES YES	O ERRORS O ERRORS
			K OHMS	NO -	YES	O ERRORS
			K OHMS	NO	YES	O ERRORS
			K OHMS	NO	YES	O ERRORS O ERRORS
			מווותט א	110	1123 	O ENNUND
X						
				na lama sa		
OTO	TOLA IN	C. SIZE	CODE IDENT	NU. JDWG NO		
	Electronics Divis		94990		12-P13'	<b>72</b> 1D
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SCALE

8/N	05	•	DAT	re of test _	5/27/75
		1.		STED BY	
		•	• • •		
• • • • • • • • • • • • • • • • • • •	*		•	(E) TEST	LIMITS
8.3.3	TIME 11:30	•	•		
. O 4	AO WINIMPO	v ome	•	•	
8.4	50 MINUTES				
	60 MINUTES 4.5	<del>-</del>		**************************************	
<b>J</b>	70 MINUTES 1.47			• •	
Ť	80 MINUTES 1,4	43 K OHMS	% CHANGE		
	90 MINUTES	K OHMS	% CHANGE	:1	
1	e i u uorman	I HAT VOI MO	's w worms	or <i>Earl</i> vo	me
*	-6.1 V VOLTAGE		·		irs .
	-6.1 V CURRENT				
	-6.1 V POWER 40	•			
			A A A B		
	TOTAL MEMORY ID	E POWER 102	.7228 mw	•	170 mw MAX
1		•	7228 mw		170 mw MAX
8.4.2	DID AN ERROR OCC	•	7228 mw		170 mw MAX
8.4.2	DID AN ERROR OCC	CUR?	<u>7228</u> mw		170 mw MAX
8.4.2	DID AN ERROR OCC	•	7228 mw		O ERRORS
8.4.2	DID AN ERROR OCC NO X YES AI	ODRESS	BIT		• O ERRORS
<b>51</b>	DID AN ERROR OCC NO X YES AI -6.1 V VOLTAGE	ODRESS /	BIT	—— Е <u>5,25</u> volt	• O ERRORS
<b>31</b>	DID AN ERROR OCC NO X YES AI -6.1 V VOLTAGE -6.1 V CURRENT	ODRESS / C.406 VOLTS 255 ma	BIT +5 V VOLTAG +5 V VOLTAG	E <u>5,25</u> VOLT E <u>760</u> ma	• O ERRORS
<b>31</b>	DID AN ERROR OCC  NO X  YES AI  -6.1 V VOLTAGE  -6.1 V CURRENT  -6.1 V POWER	ODRESS / C.406 VOLTS 255 ma 633,53 mw	+5 V VOLTAG +5 V VOLTAG +5 V POWER	E <u>5,25</u> VOLT E <u>760</u> ma 3990.8 mw	O ERRORS
<b>31</b>	DID AN ERROR OCC NO X YES AI -6.1 V VOLTAGE -6.1 V CURRENT	ODRESS / C.406 VOLTS 255 ma 633,53 mw	+5 V VOLTAG +5 V VOLTAG +5 V POWER	E <u>5,25</u> VOLT E <u>760</u> ma 3990.8 mw	• O ERRORS
<b>31</b>	DID AN ERROR OCC  NO X  YES AI  -6.1 V VOLTAGE  -6.1 V CURRENT  -6.1 V POWER	CUR?  C1406 VOLTS  255 ma  633,53 mw  ERATING POWE	+5 V VOLTAG +5 V VOLTAG +5 V POWER	E <u>5,25</u> VOLT E <u>760</u> ma 3990.8 mw	O ERRORS
8.4.2	DID AN ERROR OCC  NO X  YES AI  -6.1 V VOLTAGE  -6.1 V CURRENT  -6.1 V POWER  TOTAL MEMORY OPI  WC a) DID AN ER	CUR?  C1406 VOLTS  255 ma  633,53 mw  ERATING POWE	+5 V VOLTAG +5 V VOLTAG +5 V POWER	E <u>5,25</u> VOLT E <u>760</u> ma 3990.8 mw	O ERRORS
<b>31</b>	DID AN ERROR OCC  NO X  YES AI  -6.1 V VOLTAGE  -6.1 V CURRENT  -6.1 V POWER  TOTAL MEMORY OPE  WC a) DID AN ERROR  NO X	CUR?  C.406 VOLTS  255 ma  633,53 mw  ERATING POWE	+5 V VOLTAG +5 V VOLTAG +5 V POWER R 5323.53	E <u>5,25</u> VOLT E <u>760</u> ma 3990.8 mw	O ERRORS
<b>31</b>	DID AN ERROR OCC  NO X  YES AI  -6.1 V VOLTAGE  -6.1 V CURRENT  -6.1 V POWER  TOTAL MEMORY OPE  WC a) DID AN ERROR  NO X	CUR?  C1406 VOLTS  255 ma  633,53 mw  ERATING POWE	+5 V VOLTAG +5 V VOLTAG +5 V POWER	E <u>5,25</u> VOLT E <u>760</u> ma 3990.8 mw	O ERRORS 7000 mw MAX O ERRORS
8.4.4	DID AN ERROR OCC  NO X  YES AI  -6.1 V VOLTAGE  -6.1 V CURRENT  -6.1 V POWER  TOTAL MEMORY OP  WC a) DID AN ERROR  NO X  YES AI	CUR?  CORESS  C.406 VOLTS  255 ma  633.53 mw  ERATING POWE  ROR OCCUR?	+5 V VOLTAG +5 V VOLTAG +5 V POWER R 5323.53	E <u>5,25</u> VOLT E <u>760</u> ma 3990.8 mw	O ERRORS
8.4.4	DID AN ERROR OCC  NO X  YES AI  -6.1 V VOLTAGE  -6.1 V CURRENT  -6.1 V POWER  TOTAL MEMORY OPE  WC a) DID AN ERROR  NO X	CUR?  CORESS  C.406 VOLTS  255 ma  633.53 mw  ERATING POWE  ROR OCCUR?	BIT  +5 V VOLTAG  +5 V VOLTAG  +5 V POWER  R 5323.53  BIT  NT NO. DWG NO.	E <u>5,25</u> VOLT E <u>760</u> ma 3990.8 mw	O ERRORS 7000 mw MAX O ERRORS

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•	5/N	105	•	•	•	DATE OF TEST	5/27/75	1
			•	•		TESTED BY	The Clar	
	8.4.4	(Cont.)		•			LIMITS	The Constant of the Constant o
		WC b) DID AN	ERROR O	CCUR?	eren eren eren eren eren eren eren eren			
		NO X						•
	•	YES	ADDRES	5	BIT		O ERRORS	
•	• 1.	WC c) DID AN	ERROR O	CCUR?				
		NO X		1				
		YES	ADDRES	5	ВІТ		O ERRORS	
		WC d) DID AN	ERROR O	CCUR ?				
		NO X				• •		***************************************
		YES	ADDRES	<b>S</b>	BIT		O ERRORS	*1
	8.4.6	WC a) DID AN			•			
		NO X	ADDRES	s	BI1		O ERRORS	6
		WC b) DID AN	2					
		NO _X_	ADDRES	s	BI1		O ERRORS	
	en e	WC c) DID AN	ERROR O	CCUR?				
		YES	ADDRES	s	' BI1		O ERRORS	
		WC d) DID AN	ERROR O	CCUR?				
		NO X YES	ADDRES	s	Bľ		O ERRORS	
	8.4.7	DID AN ERROR	OCCUR?					2.1
		жо <u>х</u>						
		YES	ADDRES	S	BI'		O ERRORS	-3
		· ·						9
 A	AOTO	POLA INC	SIZE	CODE IDE	NT NO. DWG N	10.		1
		lectronics Division		9499	90	12-P137	721D	
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	<del>dia no anti-propriate de la constantidad de la con</del>	Date of Test 5/19/	
	W74		• . • . • . • . • . • . • . • . • . • .
· L	VACUUM TEST COMMY 1 8 1914	Limits	
9.	My , ~		in de la companya di dia dia dia dia dia dia dia dia dia
9.2	Did Any Bit Errors Occur?		• • • • • • • • • • • • • • • • • • •
	No ~	• • • • • • • • • • • • • • • • • • • •	
•	Yes Address Bits	0 Erro	rs
.2.1	Fast Decompression		
	Date 5/19/75 Tested by	2001	
	3/13/13		
•	Did Any Bit Errors Occur?	. :1	
	No		
	Yes Address Bits	0 Erro	rs
		•	
9.2.2	Hard Vacuum		
e ja sasar K	Parts of h	Le Contraction	60 HAY 19 18
	Date 419/25 Tested by	and the	W HYA 3 Y
	Did Any Bit Errors Occur?		
	No		
	Yes Address	Bits O Erro	ors
			(B)
10.	VIBRATION TEST	( ) A	1974
	Date 5.21.75 Tested by	retail '	MAY 1 9
		MAY 2 1 1974	GER!
	SINE SWEEP		
	Axis X - Did Any Bit Errors Occu	1 <b>r?</b>	
	No L		
	Yes Freq Address	BitsO Erro	ors

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	8/N 105	•			st 5-21-75	
	Axis Y - Did Any E	Bit Er		,	Limits	
	Yes Freq	A	ddress	Bits	0 Errors	
	Axis Z - Did Any	Bit E	rrors Occur?			
	Yes Freq	Ad	dress	Bits	0 Errors	1995
	RANDOM VIBRATION					***
	Axis X - Did Any	Bit E	rrors Occur?			****
	No L					
	Yes Freq	Ad	dress	Bits	_ 0 Errors	
	Axis Y - Did Any	Bit E	rrors Occur?			
	No			•		
	Yes Freq	Ad	dress	Bits	0 Errors	ET E
		D44 79			and program of the second of t	**
	Axis Z - Did Any	BIT E	rrors Occury		MY 5 1 Ja	74 7
1 • 1 •	Yes Freq		dwana	Dita	_ //	
	fee tred	<b>,                                 </b>	dress	DICS	- Carora	y 1
11.	SHOCK TEST			50 N	NAY 1 81975	
	Date 5/16/5		Tested By	الماعا		3 %
	6 MILLISECOND DUR	AT TON	SHOCK			1
	Y Direction - Did			cur?		
	No L_	,,,,,,				
	Yes Address	<b>.</b>	Bits		0 Errors	
MOT		SIZE	CODE IDENT NO.	DWG NO.		
	OROLA INC. ent Electronics Division	A	94990		12-P13721D	
**************************************	201 E. McDOWELL ROAD TTSDALE, ARIZONA 85252			ON	SHEET 22	- * 1.0.0
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8/N_	105	Dat	te of Test	
			,	Limits MAY 16197
Z Dir	ection - Did Any	Bit Errors Occur?	( Asia)	
		•	(C.4.8)	
*	•	Bits		0 Errors
•			•	
	· · · · · · · · · · · · · · · · · · ·	Bit Errors Occur?	•	
No		Bits		
Yes _	Address	Bits		0 Errors
12 M	ILLISECOND DURATIO	ON SHOCK		
<b>Y</b> Dia	rection - Did Any	Bit Errors Occur?		
Жо				
Yes _	Address	Bits		0 Errors
7 D4	eation - Did inv	Bit Errors Occur?		
%о		BIC EFFORM OCCULY		
		Bits		0 Errors
	entitles	, , ,		
X Dii	rection - Did Any	Bit Errors Occur?		
<b>%</b>	<u>~</u>		•	
Yes _	Address	Bits		0 Errors
				MAY 1 8 1978(A) "
	사람이 발표한 경험을 보고 있다고 있다. 기업으로 된 경험을 가고 있다.			
	고기에 가게 말하는데 있는다. 기타 기계			
MOTORO	A INC SIZE	CODE IDENT NO. DWG NO.		
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SCOTTSDALE, ARIZONA 85252

SCALE

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SHEET 23

Date of Test 5/27/75

Tested By_

7.4	CHASSIS ISOLATION  Impedance 29 meg 1	<u>Limit</u> ≥ 9 megohms
7.5	INPUT SIGNAL LOADING	
7.5.2	Current from INITIATE PULSE to Gnd 1.104 ma	≤ 2 ma
•	Current from 2.4V to INITIATE PULSE .90 pa	≥ 20 µa
7.5.3	Current from MEM SEL 1 to Gnd 1,102 ma	∠ 2 ma
	Current from 2.4V to MEM SEL 1	≤ 20 μ a
7.5.4	Current from MEM SEL 2 to Gnd 1,105 ma	≤ 2 ma
	Current from 2.4V to MEM SEL 2	≤ 20 µa
	Current from MEM SEL 3 to Gnd	≤ 2 ma
•	Current from 2.4V to MEL SEL 3 .93 ya	≤ 20 µ a
	Current from MEM SEL 4 to Gndma	≤ 2 ma
•	Current from 2.4V to MEM SEL 4	≤20 p a
7.5.5	Current from READ/WRITE to Gnd	≤ 2 ma
	Current from 2.4V to READ/WRITE /.59	≥ 20 µa
7.5.6	Current from ADDRESS 2° to Gnd	≤ 2 ma
	Current from 2.4V to ADDRESS 20 5.85 pa	≥20 ya

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8701 E. McDOWELL RUAD SCOTTSDALE, ARIZONA 85252

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8/N 105

Date of Test 5/27/75
Tosted By

			<b>.</b>			Limits
Current	from	ADDRESS	2 to Gnd _	:932 ma		≰ 2 ma
Current	from	2.4V to	ADDRESS 21_	5,42 ya		≤ 20 Ha
Current	from	ADDRESS	2 ² to Gnd	1.009 ma	: • · · · · · ·	<b>€ 2</b> ma
Current	from	2.4V to	ADDRESS 22	6.44 pa		≤ 20 µ, a
Current	from	ADDRESS	2 ³ to Gnd _	,932 ma	•	≤ 2 ma
Current	from	2.4V to	ADDRESS 23_	6,82 pa		≤ 20 _/ a
Current	from	ADDRESS	2 ⁴ to Gnd _	,986ma		≤ 2 ma
Current	from	2.4V to	ADDRESS 24	7.61,2	•	420 µa

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8/N	105	

Date of Test Tested By

Limits

Current from 2.4V to	the state of the s	= 2 ma = 20 \mu a
Current from ADDRESS Current from 2.4V to		∠ 2 ma ∠ 20ع
	2 ⁷ to Gnd .997 ma ADDRESS 2 ⁷ 6.79 Na	≤ 2 ma <u> </u>
Current from ADDRESS Current from 2.4V to	28 to Gnd 1,030 ma ADDRESS 28 1,63 µ a	∠ 2 ma     ∠ 20 Na
Current from ADDRESS Current from 2.4V to		∠ 2 ma ≤ 20 µa
Current from ADDRESS Current from 2.4V to	2 ¹⁰ to Gnd 1902 ma ADDRESS 2 ¹⁰ 1164 μa	ك 2 ma ك 20 سك €
Current from ADDRESS Current from 2.4V to	2 ¹¹ to Gnd .898 ma ADDRESS 2 ¹¹ . 166 µa	≤ 2 ma ≤ 20 µa
Current from DATA IN	BIT 0 to Gnd 1,037ma	≟ 2 ma

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SIZE

CODE IDENT NO. DIG NO.

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* SCOTTSUALE, ARIZONA 85252

REVISION SCALE

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Date of Test 5/27/75
Tested By

				Limits
Current	from DATA	IN	BIT 1 to Gnd 1.030 ma	<b>≤</b> 2 ma
Current	from 2.4V	to	DATA IN BIT 1 6.97 pa	≥20 µa
Current	from DATA	TN	BIT 2 to Gnd	∠ 2 ma
			DATA IN BIT 2 7.21 µa	€ 20/ a
		•		
Current	from DATA	IN	BIT 3 to Gnd 1.020 ma.	≤ 2 ma
Current	from 2.4V	7 to	DATA IN BIT 3 3,30 pa	≤ 20/Pa
Current	from DATA	NI N	BIT 4 to Gnd	<u>∠</u> 2 ma
Current	from 2.4V	7 to	DATA IN BIT 4 7,30 Ma	€ 20/Ua
Current	from DATA	·	BIT 5 to Gnd ma	<u> </u>
		•	DATA IN BIT 5 7.57 Ma	ع در 20 <u>ک</u>
			BIT 6 to Gnd	≤ 2 ma
Current	from 2.4V	7 to	DATA IN BIT 6 5.57 µ2	≤20,2
Current	from DATA	IN	BIT 7 to Gnd	<u> </u>
			DATA IN BIT 7 5.60 pa	
				≤20/2a
Current	from DATA	IN	BIT 8 to Gnd	<u></u> 2 ma
Current	from 2.4	7 to	DATA IN BIT'S 5.92 Ma	ع مر 20 🗠
Current	from DATA	IN	BIT 9 to Gnd	<u>≤</u> 2 ma
			DATA IN BIT 9 6.05 µ2	عر 20 کے
			and the second control of the second control	

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SIZE | CODE IDENT NO. DWG NO.

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8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

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Date of Tost 5/27/75
Tested By

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	Limits	
Current from DATA IN BIT 10 to Gnd 962 ma  Current from 2.4V to DATA IN BIT 10 6.03 Na	∠ 2 ma ∠ 20µa	
Current from DATA IN BIT 11 to Gnd .972 ma	∠ 2 ma	
Current from 2.4V to DATA IN BIT 11 6.07 Pa	∠ 20µ2	
Current from DATA IN BIT 12 to Gnd 983 ma  Current from 2.4V to DATA IN BIT 12 5.65 Na	∠ 2 ma ∠ 20µa	
Current from DATA IN BIT 13 to Gnd 984 ma	≤ 2 ma	
Current from 2.4V to DATA IN BIT 14 5,69 pa	∠ 20µa	
Current from DATA IN BIT 14 to Gnd	∠ 2 ma	
Current from 2.4V to DATA IN BIT 14 5.4/ pla	عر20 <u>ح</u> 2 ma	
Current from DATA IN BIT 15 to Gnd	€ 20µa	
Current from DATA IN BIT 16 to Gnd ma	£ 2 ma	
Current from 2.4V to DATA IN BIT 17 4,70 pa	≥ 20 µa	
Current from DATA IN BIT 17 to Gnd	∠ 2 ma ∠20µa	
가 하는 것이 되었다. 그는 사람들은 사람들은 사람들이 되었다. 그는 사람들이 되었다. 그런 사람들이 되었다. 그런 사람들이 되었다. 그 사람들은 물론 사람들은 사람들은 사람들이 되었다. 그런 사람들이 가지 않는 것이 되었다. 그는 것이 되었다. 그런 것이 되었다.	19 - 20 - 20 1 1 2 1 2 2 2 2 2 2 2 2 2 2 2 2 2 2	

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Date of Test 5/27/76

Tested By

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7.6	VERIFICATION OF OPEN COLLECTOR	ON OUTPUT SIGNAL	<u> </u>
7.6.3	READ COMPLETE voltage 50	my	<b>€</b> 100 mv
7.8.4	DATA OUT BIT 0 voltage 20	my	≤ 100 mv
	DATA OUT BIT 1 voltage	mv	≤ 100 mv
	DATA OUT BIT 2 voltage	mv	≤ 100 mv
	DATA OUT BIT 3 VoltageO	mv	≤ 100 mv
	DATA OUT BIT 4 voltage	mv	≤ 100 mv
	DATA OUT BIT 5 voltage	mv	<b>≤</b> 100 mv
	DATA OUT BIT 6 voltage 5	mv	≤ 100 mv
	DATA OUT BIT 7 voltage	mv	≤ 100 mv
	DATA OUT BIT 8 voltage O	mv	≤ 100 mv
	DATA OUT BIT 9 voltage	mv	<b>≤</b> 100 mv
	DATA OUT BIT 10 voltage 10	mv	≤ 100 mv
	DATA OUT BIT 11 voltage	my	≤ 100 mv
	DATA OUT BIT 12 voltage	mv	≤100 mv
	DATA OUT BIT 13 voltage	mv	<b>∴ 100</b> mv
	DATA OUT BIT 14 voltage 15		<b>≤</b> 100 mv
	DATA OUT BIT 15 voltage 10	mv	≤100 mv
	DATA OUT BIT 16 voltage 5	my	<b>≤100 mv</b>
	DATA OUT BIT 17 voltage 10	my	₹ 100 mv
<b>高</b> 套		いっこうしょも だいしょうだん おいちょく しょうかん かんりょう	

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CODE IDENT NO. DWG NO.

8/N 105

Date of Test 5:27.75 Tested By

Limits

POWER CONSUMPTION (25°C) 7.7

Memory +5V Voltage _5,000 7.7.1 Giolts 6,102 V CLS Memory -6.1V voltage +0.1 10.1 +5V Current

50.5 +5V Power

3,2 ch5 Memory -6.1V Current 6.102 ma 7.7.2

Memory -6.1V Power /7.5264 mw

Total Memory Idle Power 70,02mw 170 mw max 7.7.3

Memory +5V Voltage 5.00 / Volts 7.7.5

Memory -6.1 V Voltage 6,107 Volts

5350.47 +5V Power

Memory -6.1V Current 2/5 7.7.8

Total Active Power 6663.675 7.7.7

READ COMPLETE TIMING 7.8

+5V Current.

Delay 405 7.8.5

Duration 330

7000 mw max.

500 ns max.

250 ns min

450 ns max.

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8/N 105	

Date of Test 5/27/75

LIMITS

7.8.7	READ CO	MPLETE/DATA OUTPUT	TIMING
7.8.8	<b>DO-</b> O	OKREJECT	
	DO-1	OKREJECT	
	DO-2	OKREJECT	
	DO-3	OKREJECT	•
•	DO-4	OKREJECT	
	DO-5	OKREJECT	
• 1	DO-6	OKREJECT	:
	DO-7	OKREJECT	•
	DO-8	OKREJECT	
	DO-9	OKREJECT	
	DO-10	OKREJECT	
	DO-11	OKREJECT	
	DO-12	OKREJECT	•
	DO-13	OKREJECT	
	D0-14	OKREJECT	
	D0-15	OKREJECT	
	DO-16	OK PRIECT	•

REFER TO TEST PROC.

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SCALE

CODE IDENT NO. DWG NO. 94990

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	B/N 165		Date of Tost 5/27/75	
			Limits	Ī
7.9	SYSTEM FUNCTIONAL	TEST		
7.9.2	Did an error occur			ĺ
	Yes Address	Bits	0 errors	
7.9.4	Did an error occur No X			•
•	Yes Address		0 errors	
7.9.10	Did an error occur			
	Yes Address	Bits	0 errors	i [
7.9.16	Did an error occu:			1
	Yes Address	Bits	0 error	
7,10	RANDOM ACCESS CAP	ABILITY		•
7.10.6	Did an error occu			
	Yes Address	Bits	0 error	8 4
7.10.7	Did an error occu		요. 경기 기본 발생이 되었다. 이 중요된다. 그렇게 되었다. 이 그리고 있는 사람들은 보이다. 그리고 있다. 이 경기를 그리고 있는 사람들은 기를 가게 되었다. 그리고 있다.	. 0
	a) No // Addre	ssBits	_ 0 error	s []
	ROLA INC.	SIZE   CODE IDENT NO. DWG A 94990	NO. 12-P13721D	

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8201 E. MCDOWELL ROAD

	8/N 105	<del></del>	10.74	Date of Test 5/23/75 Tested By
				Limit
	b) NoX_			
	Yes	A@iress	Bits	0 error
**************************************	c) No X		•	
	Yes	Address	Bits	0 error
7.11	NON-VOLATIL	TY TEST		
.11,7	Did an error	c occur?		
7.11.9	No X			
	Yes Ac	dress Bits		. 0 error
7.12	MEMORY SELEC			
				0000
	Address 000	000 (Octal)		0000
	Address 000:	000 (Octal)  1 000 (Octal) 0 000 (Octal)		<b>0</b> 000 <b>0</b> 000
	Address 000: 001:	000 (Octal)  1 000 (Octal) 0 000 (Octal) 1 000 (Octal)		0000 0000 0000
	Address 000: 001: 001:	000 (Octal)  1 <u>COO</u> (Octal)  0 <u>OOO</u> (Octal)  1 <u>DOO</u> (Octal)  0 <u>OOO</u> (Octal)		0000 0000 0000
	Address 000: 001: 001: 010: 010:	000 (Octal)  1 000 (Octal)  0 000 (Octal)  1 000 (Octal)  0 000 (Octal)  1 0000 (Octal)		0000 0000 0000 0000
	Address 000: 001: 001: 010: 010:	000 (Octal)  1 000 (Octal)  0 000 (Octal)  1 000 (Octal)  0 000 (Octal)  1 000 (Octal)  1 000 (Octal)		0000 0000 0000 0000 0000
	Address 000: 001: 000: 010: 010: 011:	000 (Octal)  1 <u>COO</u> (Octal)  1 <u>DOO</u> (Octal)		0000 0000 0000 0000 0000
	Address 000: 001: 010: 010: 011: 100:	000 (Octal)  1 000 (Octal)  0 000 (Octal)  1 000 (Octal)  0 000 (Octal)  1 000 (Octal)  1 000 (Octal)		0000 0000 0000 0000 0000

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12-P13721D

SIZE

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Yes Address Bits	NoX_				
	Yes Addr	ess Bi	ts		0 erro
는 있는 사람이 생각되었다. 한 사람들의 발표로 발표하는 사람들이 보고 하지만 하는 생각이 되는 것이 되는 것이 되었다. 그런 사람들은 학교로 하고 하는 사람들이 되었다. 그런 사람들이 되었다. 그 보다는 물로 보다는 사람들은 회문을 보는 사람들이 있다. 그는 것이 되었다. 그는 것이 되었다. 그는 것이 모든 사람들이 가지 않는 것이 되었다.					
가는 보고 있는 것이 되었다. 그는 사람들은 이 가장 아이를 보고 있다. 그런 사람들은 사람들이 되었다는 것이 되었다. 그는 사람들은 사람들이 되었다. 그는 사람들은 사람들이 사람들이 있는 것이 되었다. 그는 사람들이 되었다. 그는 사람들이 되었다. 그는 사람들이 모르는 사람들이 되었다. 그는 사람들이 되었다.					

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SIZE

GODE IDENT NO. DWG NO. 94990

12-P13721D

8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252 SCALE R

REVISION

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Limits

7.13.4	a)	Did	an	error	occur?
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No ____

Yes Address

0 errors

b) Did an error occur?

No X

Yes Address

Bit

0 errors

MOTOROLA INC.

ision A

SIZE

94990

DWG NO.

12-P13721D

8201 E, McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

SCALE REVISION

SHEET

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Project

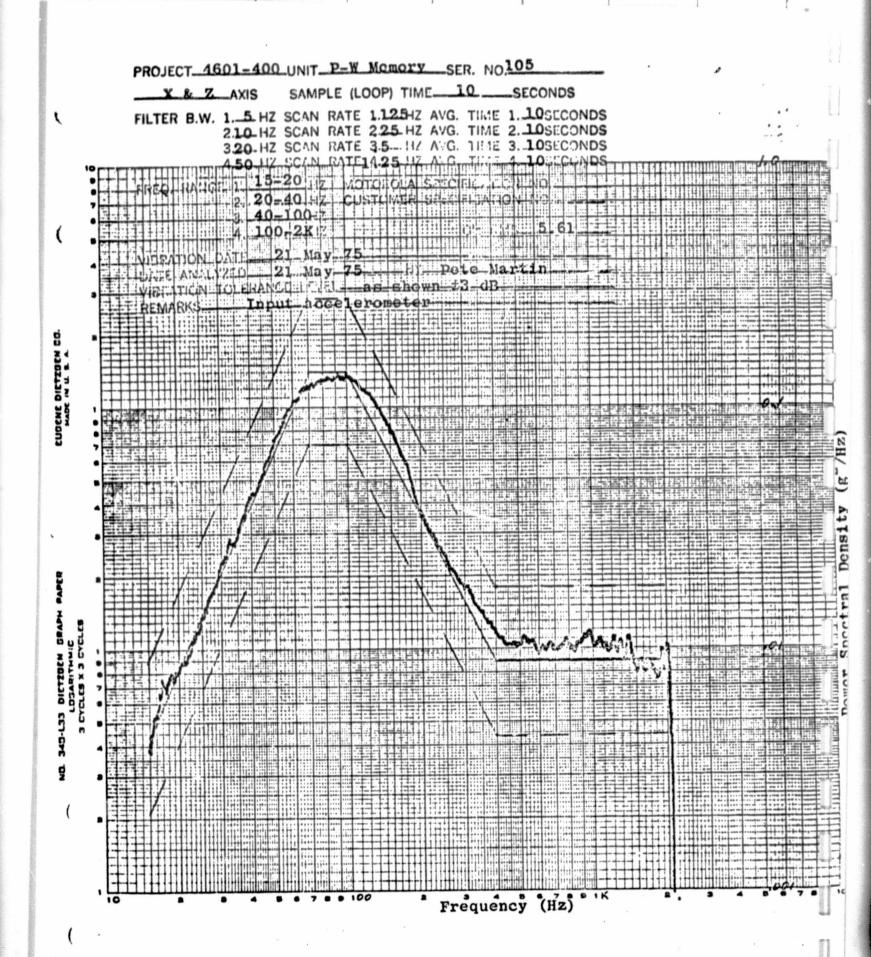
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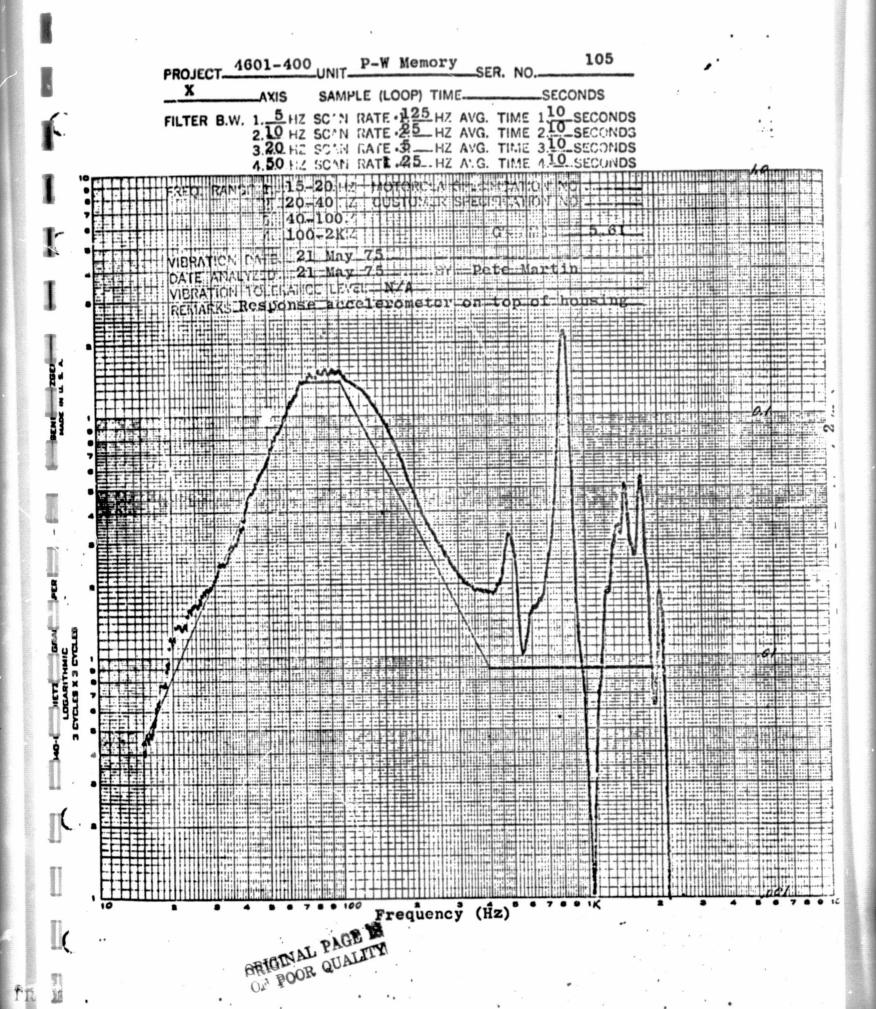
Specification Model NA HIGH VACUUM TEST Vacuum System No. CENTROL 41 W.O. 3039 PRESSURE REMARKS TIME (mm Hg A) VERT TO ATM

MOTOROLA/GED KO166 1/69

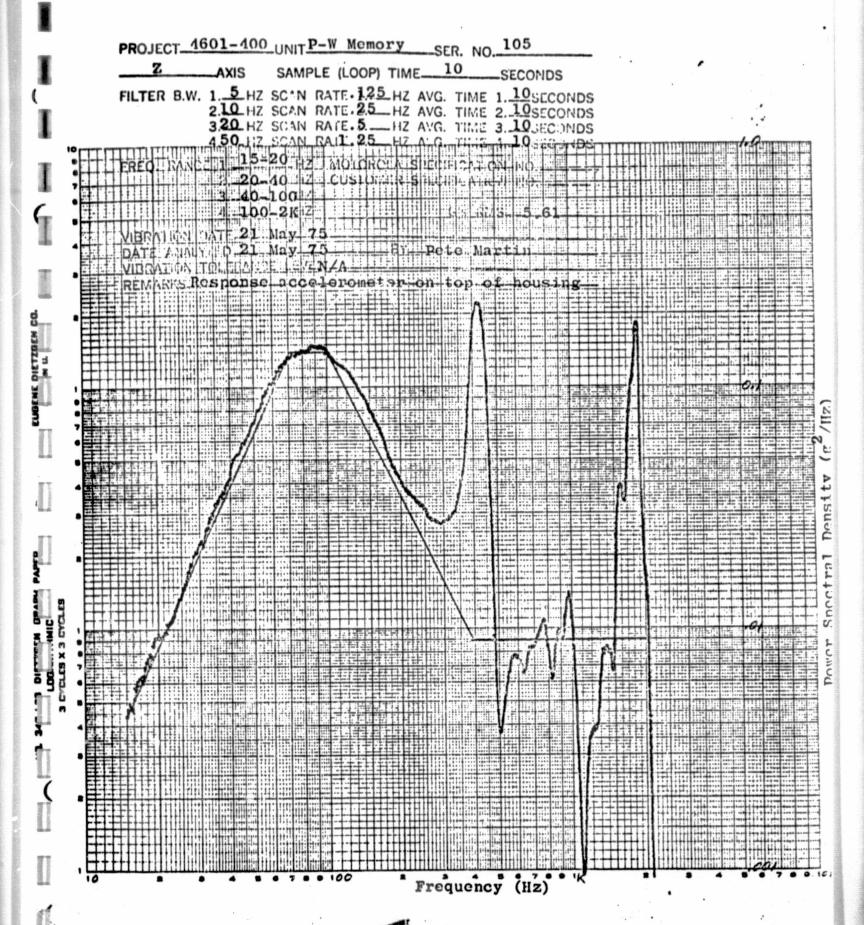
MOTOROLA INC.	VIBRATION TEST	" *
PROJECT 4/201 - 4/20	DATE 21 May 25 UNIT Plated Wire Memory	1-3
OPERATOR Peter	W.O. NO304/	z -       z
DBSERVER Lee Low	5 TO 2000 Hz	
SPEC DETAILS		x y

RUN NO.	TIME	TIME	ACCMON- Walkarder VIB. TIME	UNIT SER. NO.	DISPLACEMENT INCHES D.A.	ACCELERATION RMS PK G'8 MV (RMS)	REMARKS
Y	10:03	10'05	2411	105	NA	5.61 56.1	shaped random
Y	10.10	10:14	4.3 nw	105	. 33	19912 70435	sine sweep 5-110-2000 HZ
2	11:19	11:21	ZMIN	105	NA	3.61 36.1	chaped random
2	11:23	11:27	4.3 MIN	105	,33	109 pp 4 70 +35	sine sweep 5-110-2000 HZ
X	12:41		ZMIN	105	NA	3.61 56.1	shapee jandom
X	12:45		4.340	105	.33	104 pk 4 240 20 +35	sine sweep 5-110-2000 Hz
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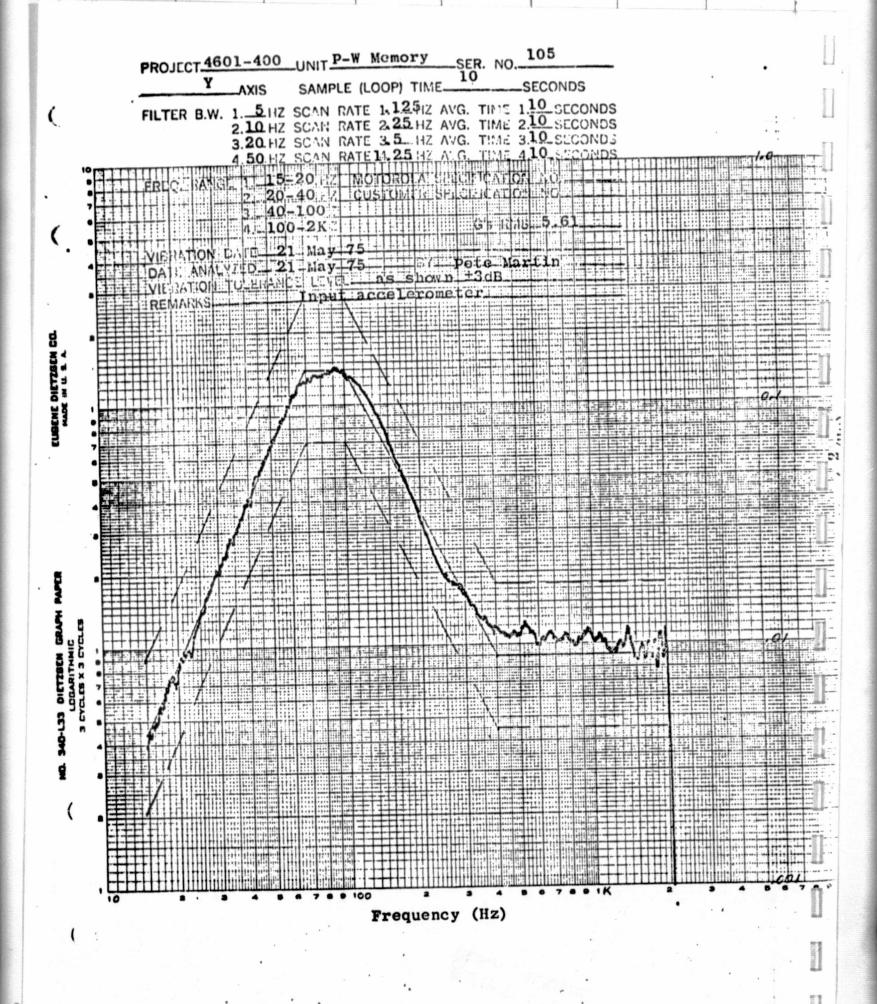




PROJECT_4601-400 UNIT_P-W_Memory_SER, NO.105 SAMPLE (LOOP) TIME____SECONDS FILTER B.W. 1. 5 HZ SCAN RATE 1.125-IZ AVG. TIME 1.10SECONDS ( 2.10 HZ SCAN RATE 2.25 HZ AVG. TIME 2.10SECONDS 3.20-HZ SCAN RATE 3.5-HZ AVC. TIME 3. 10SECONDS 450 17 SC NATE 1.25 N C T 1 10 CC N 15=20 N ACTOR A SECRETAR NO 2 20-40 CUSTOM SECRETAR NO 1 40=100-7 SC NO SECRETAR NO 1 100-2K ( NITERATION ALL 21 May 75 Pote Martin Pote Martin VIR ITION TOLLIANCE LO BE Shown ±3-dB REMARKS Input accelerometer Frequency (Hz)



ORIGINAL PAGE IN



## ATTACHMENT V

ACCEPTANCE TEST DATA SHEET
LOW POWER RANDOM ACCESS
SPACECRAFT MEMORY
PART NO. 01-P13701D
DRAWING NO. 12-P13721D
SERIAL NUMBER 106
(35 PAGES)

* APPLIC	ATION						R	EVI	SIO	NS											
EXT ASSEMBLY	USED O	N L	TR			1	DESCR	RIPTI	ON						DA	TE		AF	PR	OVE	D
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STERISK INDICATES	ORY	×	4	CI	nange	10,	17	, 19 t fr	), 3	6.0				7-	-24	1-7	3	11.	Je	ue	۵
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HEET 27 28	29 30 31	32 33 3		-	S).	) 1   X ⁴	X1 X	, , , , , , , , , , , , , , , , , , ,	X1	X1	, x6	x 6	x6	х6	x6	X1	X1	X1	xi	XI	x
HEET 27 28 EV STATUS RE	29 30 31 V x 5 x5	32 33 3 X1 X1 X		-	X1 X1 8 9	1 X4 10	-	(1 X1 2 13	_	-	-	-	_	-	+	+	-	+	-	-	•
HEET 27 28 REV STATUS RE OF SHEETS SHE	29 30 31 V x 5 x5 ET 1 2	32 33 3 X1 X1 X	4 35 1 X1	-	X1 X1 8 9	1 X4 10	-	-	_	-	-	-	_	-	+	+	-	+	-	-	-
HEET 27 28 REV STATUS RE OF SHEETS SHE	29 30 31 V x 5 x5 ET 1 2	32 33 3 X1 X1 X 3 4	4 35 1 X1 5 6	X1 7		_	11 1	-	_	-	-	-	_	-	+	+	-	+	-	-	•
HEET 27 28 REV STATUS RE OF SHEETS SHE FOR ASSOCIATED LIST	29 30 31 V x 5 x5 ET 1 2 TS SEE IN ACCORDAN PECIFIED DR RE IN E. FOR CHE	32 33 3 X1 X1 X 3 4 3 ICE WITH ST BY H.	4 35 11 X1 5 6	X1 7	RESCRI	BED B	11 1	2 13 TO	RO	15 LA	16	17 NC	18	/82	+	21 AST	22 McI	23 DOWE	24 ELL	2.5	0
HEET 27 28 REV STATUS RE OF SHEETS SHE FOR ASSOCIATED LIST WITERPRET DRAWING INCHES OTHERWISE SI ALL DIMENSIONS A INCHES AND END US	29 30 31 V x 5 x 5 ET 1 2 TS SEE IN ACCORDAN PECIFIED DR RE IN E. FOR NOTE MFC	32 33 3 X1 X1 X 3 4 3 ICE WITH ST BY H. G ITR NAS:	4 35 1 X1 5 6 ANDAR Twee	X1 7 RDS P	339 601	BED B	Y MO:	TO/ ment ACC LOW CRA	RO Elect PO FT	LA ronio WEF MEN	16 EER R	NC ivisi TES ANI Y,	18 on /	/82 SC DA'S	20 OI E COTT	AST ISDA	McI LE,	DOWE ARI	ELL ZON	2.5 ROA A 85	0
HEET 27 28 REV STATUS RE OF SHEETS SHE FOR ASSOCIATED LIST HTERPRET DRAWING INCHES OTHERWISE SI ALL DIMENSIONS A INCHES AND END US TOLERANCES SEE	29 30 31 V x 5 x5 ET 1 2 TS SEE IN ACCORDAN PECIFIED DR RE IN E. FOR NOTE MFC	32 33 3 X1 X1 X 3 4 3 CE WITH ST BY H. GBY TR NAS: EASE	4 35 1 X1 5 6 ANDAR Twee	X1 7 RDS P	339 601	BED B	11 1 Y	TO/ment ACC LOW CRA	RO Elect PO FT	LA ronio MEN MEN	16 EER R	NC ivisi TES ANI Y,	18 on /	/82 SC DA'S	20 M1 E COTT	AST ISDA	McI ALE, SI	DOWE ARI	24 ELL ZON E- 370	2.5 ROA A 85	0

SCOPE This test data sheet is to be used to record data as required by the Acceptance Test Procedure for the Low Power Random Access Spacecraft Memory. REFERENCE INFORMATION 2. 2.1 SPECIFICATIONS APPLICABLE Low Power Random Access Spacecraft S-562-P-24 Memory 12-P13722D Acceptance Test Procedure, Low Power Random Access Spacecraft Memory TEST DATA 3. Unit 8/N | O(0 Start Date of Tests Tested by ATP PARA. NO. 3.1 EQUIVALENT TEST EQUIPMENT 428A HP DCMILLIAMP METER FIJUA DIG MULITMETER FLUKE 5245L HP COUNTER PHYSICAL CHARACTERISTICS Limit WE IGHT -6.5 pounds (aluminum) Weight of LP-RASM - 5.58 Pounds

Government Electronics Division

8201 F. McDOWELL ROAD
SCOTTSUALE, ARIZONA 85252

SCALE REVISION

SIZE CODE IDENT NO. DWG NO.

12-P13721D

SHEET 2

5.8 pounds_(magnesium)

8/N 106

6.2

DIMENSIONS (

H - 12903 inches

W - <u>8.633</u> inches

MW- <u>8.964</u> inches

D - 4.320 inches

MD- 6.971 inches

V - H X W X D - 158.4 inches

Limit



≤ 160 inches³



MOTORIOLA INC.

Government Electronics Division

8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA \$5252 SIZE

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SCALE

CODE IDENT NO. DWG NO.

94990

12-P13721D

REVISION

		ested By	06-17-75
7.4	CHASSIS ISOLATION		Limit @
	Impedance $\geq 10  \text{M}$		≥ 9 megohms
7.5	INPUT SIGNAL LOADING		
7.5.2	Current from INITIATE PULSE to Gnd 1	15ma	≤ 2 ma
	Current from 2.4V to INITIATE PULSE 4	95µa	≥ 20 µa
7.5.3	Current from MEM SEL 1 to Gnd 1.15	ma	≤ 2 ma.
	Current from 2.4V to MEM SEL 1 7(	) µa	≤ 20 µ a
7.5.4	Current from MEM SEL 2 to Gnd	o ma	≤ 2 ma
	Current from 2.4V to MEM SEL 2	ya	≤ 20 µa
	Current from MEM SEL 3 to Gnd		≤ 2 ma
	Current from 2.4V to MEL SEL 3 . 9	8 ya	≤ 20 µ a
	Current from MEM SEL 4 to Gnd	ma	≤ 2 ma
	Current from 2.4V to MEM SEL 4	O pa	≤ 20 µ a
7.5.5	Current from READ/WRITE to Gnd	<u> </u>	≤ 2 ma
	Current from 2.4V to READ/WRITE 3/0	dya	≥20µa
7.5.6	Current from ADDRESS 20 to Gnd	<u> </u>	≤ 2 ma
	Current from 2.4V to ADDRESS 20	) 4 pa	≤20 ya

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Government Electronics Division

SIZE CODE IDENT NO. DWG NO.

94990 A

12-P13721D

8701 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

REVISION SCALE

		Limits C
Current from ADDRESS	$2^1$ to Gnd $94$ ma	≤ 2 ma
Current from 2.4V to	ADDRESS 21 6.52 ya	≤ 20 µa
Current from ADDRESS		≤ 2 ma
Current from 2.4V to	ADDRESS 22 7.62 pa	≤ 20 µ a
Current from ADDRESS	` .	<b>≤ 2 ma</b>
Current from 2.4V to	Address 23 1904 pa	≤ 20 _µ a
Current from ADDRESS	24 to Gnd _ 99 ma	<b>\$2 ma</b>
Current from 2.4V to	ADDRESS 249.36 pa	هر 20 ي



MOTOFIOLA INC.
Government Electronics Division

SIZE

CODE IDENT NO. DWG NO.

REVISION

94990 A

12-P13721D

\$701 E. McDOWELL ROAD SCOTISDALE, ARIZONA 85252

2 A LUM WEAR LA DWG FORMAT

SCALE

SHEET

5

106

Tested By

			2 ⁵ to Gnd	4,95 µa	Limits  2 ma  20/0a	
Current	from	ADDRESS	2 ⁶ to Gnd _	,	ے 2 ma ≤ 20سء	: :

		27 to Gnd ma	<b>≤</b> 2 ma
Current	from 2.4V to	ADDRESS 27 5.42 ma	∠ 20/Ua
Current	from ADDRESS	$2^8$ to Gnd $\frac{1}{1000}$ ma	∠ 2 ma
Current	from 2.4V to	ADDRESS 28 167 µ a	∠ 20 Na
		29 to Gnd 1.02 ma	∠ 2 ma
Current	from 2.4V to	ADDRESS 29 75 µa	≥ 20 µa
	from ADDRESS		∠ 2 me
Current	from 2.4V to	ADDRESS 210 2.09 pa	ع لر 20 کے
Current	from ADDRESS	$2^{11}$ to Gnd $97$ ma	. <u>≤</u> 2 ma
Current	from 2.4V to	ADDRESS 2 ¹¹ 2./ \(\nu \)a	≥ 20 µ2
Current	from DATA IN	BIT 0 to Gnd A.S. 9 ma	<u> </u>
Current	from 2.4V to	DATA IN BIT 0 5.09 pa	= 20 pa
	Andrew Aller (1997) 1997 (1997) 1997 (1997)		

Government Electronics Division

CODE IDENT NO. DWG NO. 94990

12-P13721D

6201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

SCALE

SIZE

REVISION

	•				Limits	į
Current	from	DATA	IN	BIT 1 to Gnd ma	<b>≤</b> 2 ma	
Current	from	2.4V	to	DATA IN BIT 1 5.06 pa	≥ 20 Na	
Current	from	DATA	IN	BIT 2 to Gnd \\\ \\ \\ \\ \\ \ \ \ \ ma	<b>≤</b> 2 ma	:
		*.		DATA IN BIT 2 4.65 pa	≥ 20µa	
Current	from	DATA	IN	BIT 3 to Gnd 99 ma	<u>≤</u> 2 ma	
				DATA IN BIT 3 4,84 pa	≤ 20/Pa	
Current	from	DATA	IN	BIT 4 to Gnd 94 ma	<u>∠</u> 2 ma	
				DATA IN BIT 4 4,65 ma	€ 20/Ua	•
Current	from	DATA	·	BIT 5 to Gnd ma	∠ 2 ma	•
				DATA IN BIT 5 4.60 va	£ 20,00	
Current	from	DATA	IN	BIT 6 to Gnd 92 ma	<u>∠</u> 2 ma	
				DATA IN BIT 6 5.97 µa	€20 pra	
Current	from	DATA	IN	BIT 7 to Gnd 89 ma	∠ 2 ma	
				DATA IN BIT 7 5,80 pa	₹ 20 µa	
Current	from	DATA	IN	BIT 8 to Gnd $9/$ ma	<u> </u>	
				DATA IN BIT 8 6.26 Ma	₹20µ2	
Current	from	DATA	IN	BIT 9 to Gnd 99 man de	∠ 2 mg	
				DATA IN BIT 9 7.3	< 20 Ma	
				7.69		: 27 :
						-

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Tuovernment Electronics Division

SIZE

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CODE IDENT NO. DWG NO. 94990

12-P13721D

8201 E. MCDOWELL ROAD SCOTTSDALE, ARIZONA 85252

SCALE

REVISION

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S. - Marie .

		•	•	Limits (
Current	from DATA	IN BIT 10 to	Gnd .98 ma	∠ 2 ma
Current	from 2.4	to DATA IN B	IT 10 657 pa	£ 20/12
Current	from DAT	IN BIT 11 to	Gnd	∠ 2 ma
Current	from 2.4	to DATA IN B	IT 11 6,5/µa	20 pa
Current	from DAT	IN BIT 12 to	Gnd	<u>∠</u> 2 ma
Current	from 2.4	to DATA IN B	IT 12 6.02 Ma	∠20µa
Current	from DAT	IN BIT 13 to	Gnd95 ma	≤ 2 ma
Current	from 2.4	to DATA IN B	IT 13 6.1   Na	∠ 20/2a
Current	from DAT	IN BIT 14 to	Gnd 96 ma	∠ 2 ma
			IT 14 6,03 Na	≥ 20µa
Current	from DAT	IN BIT 15 to	Gnd ma	∠ 2 ma
			IT 15 6.54 Na	€ 20 µa
Current	from DAT	IN BIT 16 to	Gnd 96 ma	∠ 2 ma
Current	from 2.4	to DATA IN B	IT 19 7.11 Na	≥ 20 µa
Current	from DAT	IN BIT 17 to	Gnd <u>96</u> ma	∠ 2 ma
		to DATA IN B		20 pa
	and the second of the second		이 얼마가 된 이 집에 되는 그루어야 하셨다.	



 MOTOROLA INC.	SIZE	CODE IDENT NO.	DWG NO.	
Government Electronics Division		94990	12-P13721D	
8201 E. McDOWELL ROAD				
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Pp

s/n 106

Date of Test 0/17.75
Tested By

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		•	Limit	(M)
7.6	VERIFICATION OF OPEN COLLECTOR ON C	OUTPUT SIGNA	LS	W _C y
7.6.3	READ COMPLETE voltage	ny	<b>≤</b> 100 mv	And the second s
7.6.4	DATA OUT BIT 0 voltage 30 1	n <b>v</b>	≤ 100 mv	
	DATA OUT BIT 1 voltage 20 1	nv	≤ 100 mv	
	DATA OUT BIT 2 voltage	nv	≤ 100 mv	
	DATA OUT BIT 3 voltage 20	nv	≤ 100 mv	
	DATA OUT BIT 4 voltage 30	my	≤ 100 mv	•
	DATA OUT BIT 5 voltage 30	my i i	≤ 100 mv	
	DATA OUT BIT 6 voltage	<b>nv</b>	≤ 100 mv	
	DATA OUT BIT 7 voltage 30	mv	<b>≡ 100 mv</b>	
	DATA OUT BIT 8 voltage 10	m <b>v</b>	≤ 100 mv	
	DATA OUT BIT 9 voltage	mv	≤ 100 mv	
	DATA OUT BIT 10 voltage 30	m <b>v</b> -	≤ 100 mv	
	DATA OUT BIT 11 voltage 30	m <b>v</b>	≤ 100 mv	
	DATA OUT BIT 12 voltage 30	mv	≤ 100 mv=	•
	DATA OUT BIT 13 voltage 40	mv.	<b>≠ 100 mv</b>	
	DATA OUT BIT 14 voltage 30	mv	<b>≤</b> 100 mv	
	DATA OUT BIT 15 voltage 40	mv	≤ 100 mv	
	DATA OUT BIT 16 voltage 30	mv	<b>₹ 100 mv</b>	
		4		

INC. Government Electronics Division

A 94990

12-P13721D

8201 E. McDOWELL ROAD SCOTTSDALL, ARIZONA 85252

SCALE

SIZE

DATA OUT BIT 17 voltage

REVISION

CODE IDENT NO. DWG NO.

SHEET .

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•	s/n 106	Date of Test 06-17-7
•	3/11	Tested By
		Limits
7.7	POWER CONSUMPTION (25°C)	
7.7.1	Memory +5V Voltage 5,003 Vol	
	Memory -6.1V voltage $\frac{0.00}{0.0}$ Vol+5V Current $\frac{10.0}{50.03}$ ma +5V Power $\frac{50.03}{0.03}$ mw	
7.7.2	Memory -6.1V Current 3.2 ma Memory -6.1V Power 19.53 mw	
7.7.3	Total Memory Idle Power 69.55 mw	170 mw max
7.7.5	Memory +5V Voltage <u>5.000</u> Vol Memory -6.1V Voltage <u>6.101</u> Vol +5V Current <u>670</u> ma +5V Power <u>3350</u> mw	
.7.7.6	Memory -6.1V Current 388 ma Memory -6.1V Power 1491 mw	
7.7.7	Total Active Power 4841 mw	7000 mw max
7.8	READ COMPLETE TIMING	
7.8.5	Delay 4/0 ns Duration 310 ns	500 ns max. 250 ns min 450 ns max.

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8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252 SIZE

SCALE

CODE IDENT NO. DWG NO. 94990

12-P13721D

REVISION

8/	'N N'	<u>6</u> .		Date of Te	st <u>06-17-75</u>
•				Tested by	Shilli-
•					LIMITS .
7.8.7	READ CO	MPLETE/DAT	A OUTPUT TIM	IING	<u>DIMITO</u>
7.8.8	DO-0	ok	REJECT	• •	
	DO-1	OK	REJECT		
	DO-2	OK	REJECT_		
•	DO-3	OK	REJECT_		
<b>.</b>	1.3-4	OK	REJECT_		
	DO-5	OK	REJECT_		
	DO-6	OK	REJECT_		
	DO-7	ок	REJECT		REFER TO
	DO-8	OK_	REJECT_		TEST PROC.
	DO-9	OK	REJECT		
•	DO-10	OK_ L	REJECT		
	DO-11	OK	REJECT_		
	DO-12	OK/	REJECT_		
	DO-13	OK_	REJECT_		
•	DO-14	OK/	REJECT		
	DO-15	OK	REJECT		
	DO-16	OK/	REJECT		
	DO-17	OK_	REJECT		
	•				
	PROLA			IT NO. DWG NO.	10_012701N
Governmen	t Electronic	S Division	A   9499	U	12-P13721D

94990

REVISION

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\$201 E. MCDOWELL ROAD SCOTTSDALE, ARIZONA 85252

	s/n 106		Date of Te Tested By		<u>75</u>
•				Limits	
7.9	SYSTEM FUNCTIONAL TES	BT			
7.9.2	Did an error occur?				
	Yes Address	Bits		0 error	8
7.9.4	Did an error occur?				
	No Address	Bits		0 error	8
7.9.10	Did an error occur?				
	Yes Address	Bits		0 error	8
7.9.16	Did an ofror occur?				
	Yes Address	Bits		0 error	8
7.10	RANDOM ACCESS CAPABI	LITY			
7.10.6	Did an error occur?				
	Yes Address	Bits		0 error	8
7.10.7	Did an error occur?				
	Yes Address	Bits		0 error	S
SVOTO Governmen	DEPOLA INC. SIZE  nt Electronics Division A	CODE IDENT NO. DWI	G NO. 12-P1	.3721D	

PW-2.R.10016.101A-3 69 DWG FORMAT

SCOTTSDALL, ARIZONA 85252

REVISION SCALE

	Teste	Limits
	b) No	
	Yes Address Bits	0 errors
•	c) No	
	Yes Address Bits	0 errors
.11	NON-VOLATILITY TEST	
11.7	Did an error occur?	
<b>&amp;</b> 11.9	No	
	Yes Address Bits	0 errors
.12	MEMORY SELECT TEST	
.12.3	Address 0000 (Octal).	0000
12.4	Address 0001 <u>000</u> (Octal)	0000
	0010 <u>()000</u> (Octal)	0000
	0011 <u>0000</u> (Octal)	0000
	0100 <u>()()()</u> (Octal)	0000
	0101 <u>() () () (</u> (Octal)	0000
	0110 0000 (Octal)	0000
	0111 <u>0000</u> (Octal)	0000
	1000 <u>0000</u> (Octal)	0000
	1001 <u>0000</u> (Octal)	0000
	1010 ()000 (Octal)	0000

	MOTOMOLA INC.	SIZE	CODE IDENT NO.	DWG NO.	
	Government Electronics Division	Α	94990	12	-P13721D
į	8201 E. McDOWELL ROAD				
٦	SCOTTSDALE, ARIZONA 85252	SCALE	REVIS	ION	SHEET 13

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	Tested By	
		Limits
en e	Address 1011 <u>()0()0</u> (Octal)	0000
	1100 <u>6000</u> (Octal)	0000
	1101 (1000 (Octal)	0000
	1110 () () () (Octal)	0000
.12.6	Did an error occur?	
	No V	
• 1	Yes Address Bits	0 error
.13	WORST CASE PATTERN TEST	
	uniteriore de la companya de la com Companya de la companya de la compa	
.13.2	Did an error occur?	
	No V	
•	Yes Address Bits	0 error
.13.3	Did an error occur?	
	No V	
	Yes Address Bits	0 error
	승규는 내내가 되는 내가 있는 그리고 있다면 하는 사람들이 가득했다고 있다는 살았다.	
	으로 하지 않는 경기를 가고 있다. 하는 하는 그는 그리고 하는 것이 되었습니다. 그들은 이 사람들은 그는 그는 것이 되었습니다. 그렇게 하는 것이 하는 하는 것이 하는 것이 되는 것이 되는 것이 되는 것이 되었습니다. 그는 것이 되었습니다. 그런 것이 되었습니다.	
	아들 마을 것이 많이 살고 말로 있지 않는 것이 말라면 하고 있다. 그리고 그들을 살아왔다.	
	이번 아이들은 이번 말은 병원 사람들은 등 같은 학교에 있는 사람들이 나를 했다.	



MOTOROLA INC.	SIZE	CODE IDENT NO.	DWG NO.	-
Government Electronics Division		94990	12-P13721D	
8701 E. McDOWELL ROAD				
SCOTTSDALE, ARIZONA 85252	SCALE	REVIS	SION SHEET 14	

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ş'.		i	1.0	1		
S	/N	1	10	10	4	

Date of Test () /6 -Tested By

Limits

0 errors

7.13.4 a)	Did an erro	r occur?		
	No _	•		
	Yes A	ddress	Bit	0 errors
<b>b</b> )		r occur?		
	No /	ddress E	Bit	0 errors

CODE IDENT NO. DWG NO. SIZE MOTOROLA INC.
Government Electronics Division 94990 12-P13721D 8201 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252 SCALE REVISION SHEET 15

S/N	DATE OF TEST 6-24-75 TESTED BY
8.	TEMPERATURE TEST LINITS
8.2.1	TIME 0705
8,2,2	LOW TEMPERATURE
	THERMISTOR RESISTANCE
	150 MINUTES 213 K OHMS
	160 MINUTES 2 6 K OHMS % CHANGE 1, 34
	170 MINUTES 2 9 K OHMS % CHANGE
n de la companya. Espain	180 MINUTES K OHMS % CHANGE
	190 MINUTES K OHMS % CHANGE
8.2.3	DID AN ERROR OCCUR?
and the open of the second of	YES ADDRESS BITS O ERRORS
8.2.4	-6.1 V VOLTAGE 6.40 VOLTS +5 V VOLTAGE 5.25 VOLTS -6.1 V CURRENT 14.5 ma +5 V CURRENT 10.2 ma -6.1 V POWER 92.82 mw +5 V POWER 53.57 mw
	TOTAL MEMORY IDLE POWER 146. The
8.2.5	-6.1 V VOLTAGE 6.40 VOLTS +5 V VOLTAGE 5.75 VOLTS
	-6.1 V CURRENT 255 ma +5 V CURRENT 680 ma
	-6.1 V POWER /632 mw +5 V POWER 3.574/mw
	TOTAL MEMORY OPERATING POWER 5206 mw 7000 mw MAX
NOTO	ROLA INC. SIZE CODE IDENT NO. DWG NO.  Electronics Division A 94990 12-p13721D

SHEET

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8201 EAST McDOWELL ROAD SCOTTSDALE, ARIZONA 85257

SCALE

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8/N	106.			•	TE OF TEST O	6-2475
				,	SIED BI	Will)
•	•	•			•	LIMITS
8.2.6	DID AN ERROR	OCCUR?		•		
	NO V		WTV:	•		
	YES	ADDRES	S	BIT		O ERRORS
•			hers.			
8.2.8	WC a) DID AN	ERROR	OCCUR?			
	NO <u></u>					
	YES	ADDRES	S	BIT		0 ERRORS
	WC b) DID AN	FDDAD A	rctips ;			
	<i></i>	BANUR U	CON			
	NO NO			<b>.</b>		A FARARC
	YES	ADDRES	)5 	BIT		0 ERRORS
	WC c) DID AN	ERROR C	CCUR?			
	NO V		•			
	YES	ADDRES	88	BIT		0 ERRORS
		in the proof of				•
	WC d) DID AN	ERROR C	OCCUR?			
	NO <u>√</u>					
	YES /	ADDRES	s	BIT		O ERRORS
8.2.9	WC a) DID AN	ERROR C	CCUR?	,		
	NO 🗸					
	YES	ADDRES		BIT		O ERRORS
		244 242 Y				
	ROLA INC		CODE IDENT NO.	DWG NO.		
	Electronics Division	on A	94990		12-P13721	
SCOTT	AST McDOWELL ROAD SDALE, ARIZONA 85257	SCALE	REVIS	ION	ISHEE	T 17

SCALE

REVISION

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8201 EAST McDOWELL ROAD SCOTTSDALE, ARIZONA 85257 SIZE

CODE IDENT NO. DWG NO.

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12-P13721D

REVISION SCALE

8/N	
	TESTED BY
	LIMITS
8.3.3	TIME <u>//:20</u>
8.4	50 MINUTES 1,601 K OHMS
• •	60 MINUTES 1.510 K OHMS % CHANGE 5.1%
	70 MINUTES 1.450 K OHMS % CHANGE 4.0%
	80 MINUTES 1,433 K OHMS % CHANGE 1.2%
	90 MINUTES K OHMS % CHANGE
	- 100 P
8.4.1	-6.1 V VOLTAGE 6.40 VOLTS +5 V VOLTAGE 5.25 VOLTS
	-6.1 V CURRENT 8.0 ma - +5 V CURRENT 11.5 ma
	-6.1 V POWER 5 3.71 mw +5 V POWER 60.38 mw
	TOTAL MEMORY IDLE POWER 1/2.59 mw 170 mw MA
8.4.2	DID AN ERROR OCCUR?
	NO V
	YES ADDRESS BIT O ERROR
8.4.3	-6.1 V VOLTAGE 6.40 VOLTS +5 V VOLTAGE 5.25 VOLTS
	-6.1 V CURRENT 265 ma +5 V VOLTAGE 260 ma
	-6.1 V POWER ) 696.5mw +5 V POWER 3990.00
	TOTAL MEMORY OPERATING POWER 56865 mw . 7000 mw l
	불리다. 그는 그는 그는 그는 그리고 하는 그는 그는 그는 그는 그는 그는 그를 모르는 것이 없는 것이 없다.
8.4.4	WC a) DID AN ERROR OCCUR?
	YES ADDRESS BIT O ERROR
1070	ROLA INC. SIZE CODE IDENT NO. DWG NO.
vernment	Electronics Division A 94990 12-P13721D
	ST McDOWELL ROAD DALE, ARIZONA 85257 SCALE REVISION SHEET 19

5/X	106_			DATE OF TEST	6-24-75
				TESTED BY	LIVITS
8.4.4	(Cont.)				LINITS
	WC b) DID AN ER	ROR OCCUR?			١.
	NO N		•		
	YES A	ddress	BIT		O ERRORS
	WC c) DID AN ER	ROR OCCUR?			
	NO V	•	•		
	YES	DDRESS	BIT		O ERRORS
	WC d) DID AN EF	ROR OCCUR ?			
	NO V				
	YES	DDRESS	BIT _		O ERRORS
8.4.6	WC a) DID AN EI	RROR OCCUR?			•
	YES	DDRESS	BIT _		o errors
	WC b) DID AN EI	RROR OCCUR?			
	NO YES	ADDRESS	BIT _		O ERRORS
	WC c) DID AN EI	RROR OCCUR?			
	NO	ADDRESS	BIT _		O ERRORS
	WC d) DID AN EI	RROR OCCUR?			
	NO YES	ADDRESS	BIT		O ERRORS
8.4.7	DID AN ERROR O	CUR?			
	NO /				
	YES	ADDRESS	BIT		O ERRORS
MOTO	ROLA INC.	SIZE   CODE IDE	NT NO. DWG NO.		
overnment	Electronics Division	A 9499	0	12-P13721D	
8201 EA SCOTTS	AST McDOWELL ROAD DALE, AKIZONA 85257	SCALE	REVISION	SHEET	20
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	8/N 106			Date of Test 6-16.75 Tested by
		• **:		Limits
9.	VACUUM TEST	· ·	•	
9.2	Did Any Bit Err	ors Occ	ur?	
	No			
	YesAddre	ss	Bits	0 Errors
	· · · · · · · · · · · · · · · · · · ·			
9.2,1	Fast Decompress			
	Date ( 18 . 75		Tested by	A Landing
	Did Any Bit Err	ors Occ	ur?	
in the second se	No L			
		ess	Bits	0 Errors
			•	
9.2.2	Hard Vacuum	•		
		•		<u> </u>
	Date 6 . 18 . 75		Tested by	ZET Jennyl
	Did Any Bit Err	ors Occ	ur?	
	No L			
	Yes	Address	· 1	Bits 0 Errors
10.	VIBRATION TEST	•		
	Date 5 24.75	<u>-</u>	Tested by	- Linke
	SINE SWEEP			
	Axis X - Did An	Di+ 1	Insana Occi	
	AXIS A - DIG AL	y bit i	arrors occi	
	No			
	YesFre	<b>q</b>	_Address_	Bits 0 Errors
			•	
	• · · · · · · · · · · · · · · · · · · ·			
MOTOL	POLA INC.	SIZE C	DDE IDENT NO.	DYG NO.
	Electronics Division	A	94990	12-P13721D
8201 F	McDOWELI. ROAD N.L. ARIZONA 85252	SCALE	REVIS	SION SHEET 21

S/N Date of Test	<u> ( 24 - 75                                   </u>	4
Tested by	Fill.	Ĺ
Axis Y - Did Any Bit Error Occur?	<u>Limits</u>	
No	•	
Yes Freq Addres Bits	_ 0 Errors	
Axis Z - Did Any Bit Errors Occur?		
No 1	•	
Yes Freq Address Bits	0 Errors	
RANDOM VIBRATION		
Axis X - Did Any Bit Errors Occur?		3.1
No		
Yes Freq Address Bits	0 Errors	
Axis Y - Did Any Bit Errors Occur?		4,1
No		Ī
Yes Freq Address Bits	0 Errors	
Axis Z - Did Any Bit Errors Occur?		
No _		
Yes Freq Address Bits	0 Errors	
Date 6-18-75 Tested By		
	فه	
6 MILLISECOND DURATION SHOCK		L
Y Direction - Did Any Bit Errors Occur?		H
No		**
Yes Address Bits	0 Errors	
Government Electronics Division A 94990 DWG NO. 12-PI	13721D	
8201 E. McDOWELL ROAD SCOT ISDALE, ARIZONA 85252 SCALE REVISION	SHEET 22	

SCALE

REVISION

			Limits
Z Direct:	ion - Did Any Bi	t Errors Occur?	
No		•	•
Yes	Address	Bits	0 Errors
X Directi	lon - Did Any Bi	t Errors Occur?	
No		•	
Yes	Address	Bits	0 Errors
12 MILLIS	SECOND DURATION	SHOCK	
Y Direct:	lon - Did Any Bi	t Errors Occur?	
No	•		
Yes	Address	Bits	0 Errors
Z Direct	lon - Did Any Bi	t Errors Occur?	
No			
es	Address	Bits	_ 0 Evrors
	lon - Did Any Bi	t Errors Occur?	
No			
řes	Address	Bits	_ 0 Errors

KIOTO	POLA	INC.
Government	Electronics	Division

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CODE IDENT NO. DWG NO.

12-P13721D

8201 É, McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

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SCALE

SIZE

REVISION

94990

Date of Test 6 Tested By

		•
7,4	CHASSIS ISOLATION	Limit
	Impedance 710 meg 1	≥ 9 megohms
7.5	INPUT SIGNAL LOADING	
7.5.2	Current from INITIATE PULSE to Gnd 1.15 ma	≤ 2 ma
	Current from 2.4V to INITIATE PULSE 197 pa	≥.20 µa
7,5,3	Current from MEM SEL 1 to Gnd	2 ma
	Current from 2.4V to MEM SEL 1 7.68 ja	≤ 20 j.a
7.5.4	Current from MEM SEL 2 to Grd	≤ 2 ma
	Current from 2.4V to MEM SEL 2 194 ya	≤ 20 µa
•	Current from MEM SEL 3 to Gnd 1.15 ma	≤ 2 ma
	Current from 2.4V to MEL SEL 3 .96 ya	≤ 20 µ a
	Current from MEM SEL 4 to Gnd	≤ 2 ma
	Current from 2.4V to MEM SEL 4 .69 pa	≤20 µ a
7.5.5	Current from READ/WRITE to Gnd 196 ma	≤ 2 ma
	Current from 2.4V to READ/WRITE 2.02 pa	≥ 20 µa
7.5.6	Current from ADDRESS 20 to Gndma	≤ 2 ma
	Current from 2.4V to ADDRESS 20 6.99 pa	≤20 µa
	사람이 되었다. 하나 보는 사람이 살아 있는 사람이 없는 사람들이 없다.	

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CODE IDENT NO. DWG NO.

94990

12-P13721D

A201 E. L'. DOWELL ROAD

IREVISION.

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		•			• •	•	•	Limi	ts
Current	from	ADDRESS	21	to Gno	d <u>'</u>	74 ma		≤ 2 m	a
Current	irom	2 4V to	ADI	DRESS 2	21 6.	47 ya		بر 20 ≥	a
Current	from	ADDRESS	22	to Gne	d _/_	02ma		<b>≤ 2</b> m	a
Current	from	2.4V to	ADI	DRESS 2	2 ²	59 pa		£ 20 µ	a '
		ADDRESS						. <b>52</b> m	<b>a</b> ·
Current	from	2.4V to	ADI	DRESS :	2 ³ _8,	90 pa		≤ 20 p	a
Current	from	ADDRESS	24	to Gno	d	g ma		<b>≤</b> 2 m	<b>a</b>
Current	from	2.4V to	ADI	DRESS :	2 ⁴	25 pe		±20 µ	<b>a</b> .

MOTOROLA INC.
Government Electronics Division

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SIZE CODE IDENT-NO. DWG NO.

94990

12-P13721D

8701 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

SCALE

REVISION

Limits

	•	
Current from ADDRESS 25 to Gnd . 44 ma	≤ 2 ma	71
Current from 2.4V to ADDRESS 25 4.90 µa	£ 20 Na	
		5
Current from ADDRESS 26 to Gnd	∠ 2 ma	
Current from 2.4V to ADDRESS 25 6.07 pa	<u>←</u> 20 µ a	Tž.
The same and the s		177.00
OF the second control		
Current from ADDRESS 27 to Gnd 184 ma	<b>≤</b> 2 ma	
Current from 2.4V to ADDRESS 27 10.81 pa	∠ 20/Va	
Current from ADDRESS 28 to Gnd / 98 ma	∠ 2 ma	
Current from 2.4V to ADDRESS 28 4,47 pa	€ 20 Na	No. of Particular Part
Current from ADDRESS 29 to Gnd 1,93 ma	∠ 2 ma	
Current from 2.4V to ADDRESS 29 3.41 pa	≤ 20 µa	
Current from ADDRESS 2 ¹⁰ to Gnd 1.87 ma	∠ 2 ma	
Current from 2.4V to ADDRESS 210 /1.64 pa	ع لر 20 <u>ك</u>	
Current from ADDRESS 2 ¹¹ to Gnd 1.88 ma	≤ 2 ma	
Current from 2.4V to ADDRESS 211 9,25 µa	£ 20 µa	
		মান্ত্র
Current from DATA IN BIT 0 to Gnd 89 ma	∠ 2 ma	
Current from 2.4V to DATA IN BIT 0 5.05 pa	= 20 Na	## %

Government Electronics Division

SIZE

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CODE IDENT NO. DWG NO.

94990

12-P13721D

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	Limits
Current from DATA IN BIT 1 to Gnd 190 ma	<b>≤</b> 2 ma
Current from 2.4V to DATA IN BIT 1 5.04 pa	≥ 20 Ma
	∠ 2 ma
Current from DATA IN BIT 2 to Gnd ma	
Current from 2.4V to DATA IN BIT 2 4,62 pa	∠20µa
Current from DATA IN BIT 3 to Gnd 94 ma.	≤ 2 ma
Current from 2.4V to DATA IN BIT 3 482 Ma	≤ 20/2a
Current from DATA IN BIT 4 to Gnd ma	≤ 2 ma
Current from 2.4V to DATA IN BIT 4 4,63 pa	<u>د</u> 20ماa.
Current from DATA IN BIT 5 to Gnd ma	<b>∠</b> 2 ma
Current from 2.4V to DATA IN BIT 5 4,5% pa	عدر20 ع
Current from DATA IN BIT 6 to Gnd ma	∠ 2 ma
Current from 2.4V to DATA IN BIT 6 5,92 pa	<u>∠</u> 20/^a
Current from DATA IN BIT 7 to Gnd 98 ma	∠ 2 ma
Current from 2.4V to DATA IN BIT 7 5.76 pa	≤20/1a
Current from DATA IN BIT 8 to Gnd .90 ma	<u></u> ∠ 2 ma
Current from 2.4V to DATA IN BIT 8 6,20 pa	عسر20 ك
Current from DATA IN BIT 9 to Gnd .99 ma	<u>≤</u> 2 ma
Current from 2.4V to DATA IN BIT 9 7.62 µa	< 20 Na
그 사람들 그렇게 되어 이 있습니다. [1] 그는 그들이 되는 사람이 있는 사람들이 되는 사람들이 되었다. 그는 사람	

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s/n /06

Date of Test 6/25/75
Tested By

						Limits	
C	urront	from	DATA	IN	BIT 10 to Gnd .97 ma	<u>∠</u> 2 ma	•
C	urrent	from	2.4V	to	DATA IN BIT 10 6,43 µa	£ 20/12	
C	urrent	from	DATA	IN	BIT 11 to Gnd 1.01 ma	<u> </u>	
C	urrent	from	2.4V	to	DATA IN BIT 11 6.44 µa	a مر20 کے	
					BIT 12 to Gnd .95 ma	<u> </u>	
C	urrent	from	2.4V	to	DATA IN BIT 12 5.98 µa	∠20µa	
C	urrent	from	DATA	IN	BIT 13 to Gnd .75 ma	≤ 2 ma	
C	urrent	from	2.4V	to	DATA IN BIT 14 6.07 1/2	≤ 20µa.	
C	urrent	from	DATA	IN	BIT 14 to Gnd	<u>∠</u> 2 ma	
C	urrent	from	2.4V	to	DATA IN BIT 14 6,00 / a	£ 20µa	
C	urrent	from	DATA	IN	BIT 15 to Gnd 98 ma	∠ 2 ma	•
C	urrent	from	2.4V	to	DATA IN BIT 15 6,50 pa	£ 20 pa	
C	urrent	from	DATA	IN	BIT 16 to Gnd 195 ma	∠ 2 ma	•
C	urront	from	2.4V	to	DATA IN BIT 17 7.06 Na	€ 20 µa	
C	urrent	from	DATA	IN	BIT 17 to Gnd .95 ma	∠ 2 ma	
					DATA IN BIT 17 6.92 Na	∠20µa	

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CODE IDENT NO. DWG NO. 94990

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s/n 106

Date of Test 6/25/75
Tested By

## Limit

7.6	VERIFICATION OF OPEN COL	LECTOR ON	OUTPUT SIGN	IALS
7.6.3	READ COMPLETE voltage	15	mv	<b>≤</b> 100 mv
7.6.4	DATA OUT BIT 0 voltage	10	mv :	≤ 100 mv
en e	DATA OUT BIT 1 voltage		mv .	≤ 100 mv
	DATA OUT BIT 2 voltage	0	mv	≤ 100 mv
	DATA OUT BIT 3 voltage	5	mv	≤ 100 mv
	DATA OUT BIT 4 voltage	15	mv	≤ 100 mv
	DATA OUT BIT 5 voltage	15	mv	≤ 100 mv
	DATA OUT BIT 6 voltage	10	mv	≤ 100 mv
	DATA OUT BIT 7 voltage	0	mv	# 100 mv
	DATA OUT BIT 8 voltage	0	m <b>v</b>	≤ 1.00 mv
	DATA OUT BIT 9 voltage	10	mv	≤ 100 mv
<b>,</b>	DATA OUT BIT 10 voltage	15	mv	≤ 100 mv
	DATA OUT BIT 11 voltage	10	mv	≤ 100 mv
	DATA OUT BIT 12 voltage	10	mv	≤ 100 mv-
	DATA OUT BIT 13 voltage	20	mv	<b>∷ 100 mv</b>
	DATA OUT BIT 14 voltage	15	mv	≤ 100 mv
	DATA OUT BIT 15 voltage	15	mv	≤ 100 mv
	DATA OUT BIT 16 voltage	5	my .	< 100 mv
	DATA OUT BIT 17 voltage	20	mv	

MOTOFIOLA INC.
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SIZE

CODE IDENT NO. DWG NO.

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	8/N		to of Test 6/25/
		•	<u>Limits</u>
 7	POWER CONSUMPTION (25°C)		
7.1	Memory +5V Voltage +5,006	Volts .	
	Memory -6.1V voltage - 4,103	Volts .	
	+5V Current	ma	
	+5V Power <u>50.04</u>	mw	
7.2	Memory -6.1V Current 3.3	ma	
	Memory -6.1V Power 20.13	mw	
<b>7.3</b>	Total Memory Idle Power 70.19	фW	170 mw max
7.5	Memory +5V Voltage + 5,007	Volts	
	Memory -6.1 V Voltage -6.105	Volts	
	+5V Current	ma	
	+5V Power 3354.6.9	mw	
7.6	Memory -6:1V Current230	ma	
	Memory -6,17 Power 1404.15	mw	
7.7	Total Active Power 4758.84	mw	7000 mw max
.8	READ COMPLETE TIMING		
8.5	Delay 390 ns		500 ns max.
	Duration 320 ns		250 ns min
			450 ns m:.x.

8701 E. McDOWELL ROAD SCOTTSDALE, ARIZONA 85252

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					f Test	6/2
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		•	•		•	LIMIT
READ CO	MPLETE,	DATA OUTI	PUT TIMI	ng .	•	•
DO-0	OK	RE	IECT	•		
D0-1	OK	REJ	JECT		•••	
D0-2	OK	RE	JECT		•	
DO-3	ок	REJ	JECT			
D0-4	OK	REJ	JECT	·		
DO-5	OK	REJ	ECT	· ·		
DO-6	OK	REJ	JECT	•		
DO-7	ок	REJ	JECT			REFER
DO-8	OK	REJ	JECT			TEST
DO-9	OK	REJ	JECT	•		
DO-10	OK	REJ	IECT			
DO-11	ОК	REJ	FCT			
DO-12	OK	REJ	FCT			
DO-13	OK_	REJ	ECT	<u>. 1</u>		
DO-14	OK	REJ	ECT			
DO-15	OK		ECT			
DO-16	OK		ECT			
DO-17	OK	REJ	ECT			

MOTOROLA INC.

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CODE IDENT NO. DWG NO. 94990

12-P13721D

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		•		· · · · · · · · · · · · · · · · · · · ·	
					Limits
7.9	SYSTEM FUNCTIONA	L TEST			
		•			
7.9.2	Did an error occ	ur?			
	No		ing the second of the second o		
	Yes Addres	·	_ Bits		0 errors
7.9.4	Did an error occ	ur?			
	No /				
	Yes Address	•	Bits		0 errors
	• • • • • • • • • • • • • • • • • • •				
7.9.10	Did an error occ	ur?			
	No	a sura.			
	Yes Address	·	Bits		0 errors
7016	Did an error occ				
1.9.10	No No	sur r			
	Yes Address		Rita		0 errors
	Add Co.				
7.10	RANDOM ACCESS CA	\PABILI	TY		
7.10.6	Did an error occ	cur?			
	No '				
	Yes Addres	55	Bits		0 errors
<i>a</i> 10 #	Did an array oa				
7,10.7	a) No	Jul F			
		ress	Bits		0 errors
		•			
		•			
DAOTE	TOLA INC.	SIZE	CODE IDENT NO. D	WG NO.	
	t Electronics Division		94990	79	- P13 <b>721D</b>
\$20	I C. McDOWELL ROAD		•		
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REVISION

SHEET 32

SCALE

	S/N /06 Date of Te Tosted By	- Washington
		Limits
1.	b) No	•
	Yes Address Bits	0 errors
	c) No	
	Yes Address Bits	0 errors
•		
7.11	NON-VOLATILITY TEST	
7.11,7	Did an exror occur?	
7.11.9	No	
1.TT.8	Yes Address Bits	0 errors
7.12	MEMORY SELECT TEST	
7.12.3	Address 0000 (Cctal)	0000
7.12.4	Address 0001 <u>DOOD</u> (Octal)	0000
	0010 <u>0000</u> (Octal)	0000
	0011 <u>0000</u> (Octal)	0000
	0100 <u>0000</u> (Octal)	0000
	0101 <u>0000</u> (Octal)	0000
	0110 0000 (Octal)	0000
	0111 <u>0000</u> (Octal)	0000
	1000 <u>0000</u> (Octal)	0000
	1001 <u>0000</u> (Octal)	0000
	1010 <u>0000</u> (Octal)	0000
	에 크로 크리아이크리크로 생각하는 사람들이 있다. 그리고 그는 사람들은 보는 이 그리고 있어 함께 함께 하는 이 본 사용이 중에 관측을 통해하고 하는 것도록 모든 사람들은 사람들이 되었다. 이 것도록 기술을	
		고양을 하고 있는 제목 10 : 10 : 10 : 10 : 10 : 10 : 10 : 10 :

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Government Electronics Division

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CODE IDENT NO. DWG NO.

	•				•
	s/n	106		Date of Test	6/25/75
			• •	lested by	Limits
	Addross	1011 0000	(Octal)		0000
		1100 0000			0000
		1101 0000	(Octal)		0000
		1110 0000	(Octal)		. 0000
7.12.6		error occur?			
	No <u>/</u> Yes	Address	Bits		0 errors
7.13	WORST (	CASE PATTERN T	es <b>t</b>		
7.13.2	Did an	error occur?			
	No /				
	Yes	Address _	Bits		0 errors
7.13.3	. <b>Di</b> d an	error occur?			
	No L				
	Yes	Address	Bits		0 errors
Moro	MOLA	INC. SIZE	CODE IDENT NO. DWG	NO.	
Governmen	t Electronic		94990	12-P13721	ı <b>n</b>

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19 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	100 m		a mark a constant	•		. / -
	s/n	106	- Some a South St.	•	Date of To	st 6/25/
•	•		•	•		Limits
7.13.4	<b>a)</b>	Did an er	ror occur?			
		Yes	Address	Bit		0 errors
	b)		ror occur?			
		No V	Address	Bit		0 errors
			<b>&amp;</b>			
	•					
MOTO		DLA INC	<i>2</i> /4	IDENT NO. DWG	NO.	
overnmen	t Elec	tronics Divisi	on A 9	4990	12-P13	721D

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SHEET

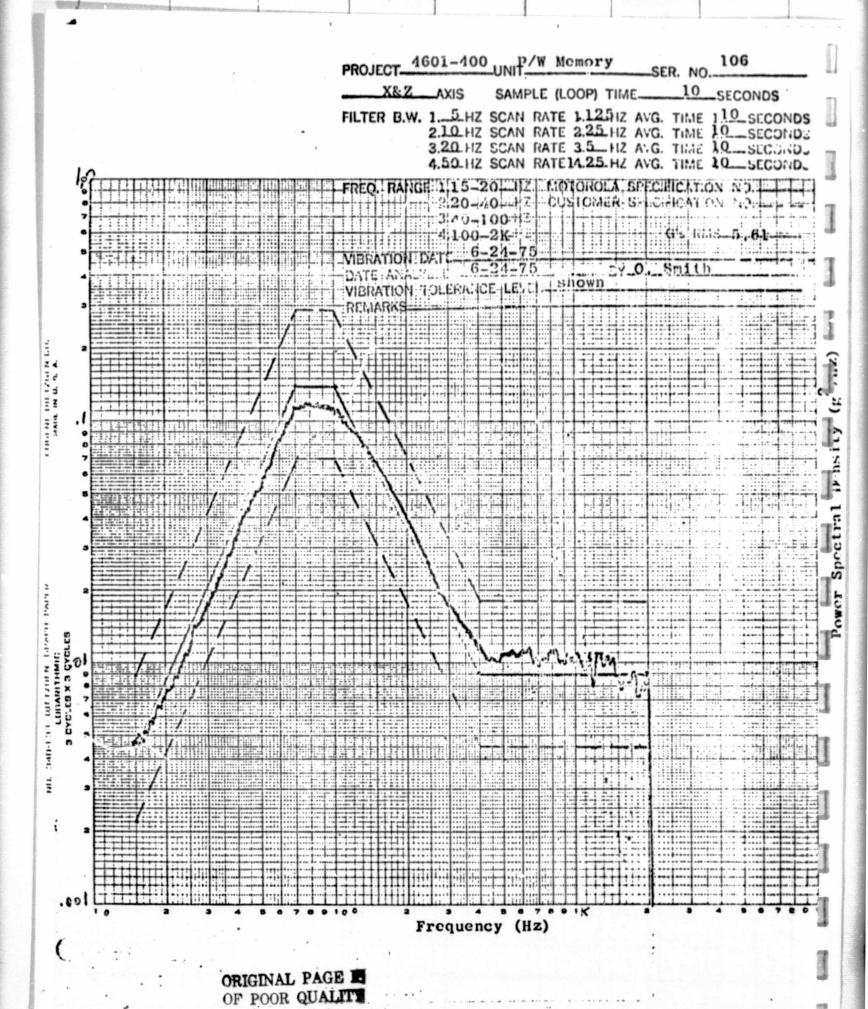
: 11

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MOTOROLA INC.	VIBRATION TEST	\ \ X
SHEETOFDATE	24-75	Y
	1. 3041 2	# 2
OBSERVER J. Joulden	TO 2 K HZRATEDON	7
SPEC DETAILS 12 - 13722		
1		X Y

tea

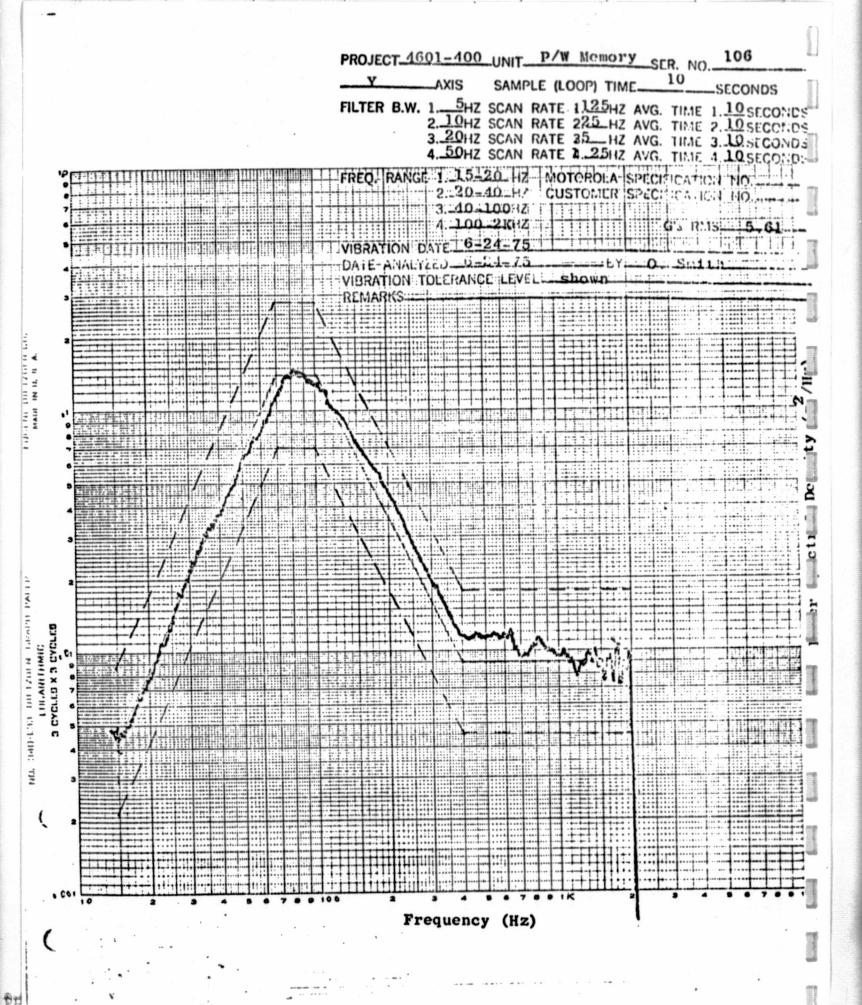
RUN NO.	TIME	TIME	ACCUM- ULATED VIB. TIME	UNIT SER. NO.	DISPLACEMENT INCHES D.A.	ACCELERATION PK	REMARKS
3	1220	7777	ani.	106	NA	5.61	RESPONSE ACCEL = . 1.5 g KMI SHAPEO RANDOM NOISE
2/2	1735	142	MIN	106	.33	10-5	5-2KHZ SINE SWEEP
13	1820	24	MIN	106	, 33	10-5	" "
4	717	840	Min	106	NA	5.6.1	RESPONSE ACCEL = 154 RNS 64 APEO RANDANI NOISE
15	2014	1:26	Min	106	NA	5.6.1	SHOWED RANDON NOISE
1	2:25	1/2	MINI	106	, 33	10.5	5 - JKHZ SINE SWEEP
						=	- Fr JEST NeSmit
15	1038	2039	375EC	106	.33	10-35	5- THE SINE SWEEP
1/8	2050	2054	1 MIN 21566	106	, 3 3	10-35	5-2KHZ " "
							ENO TEST
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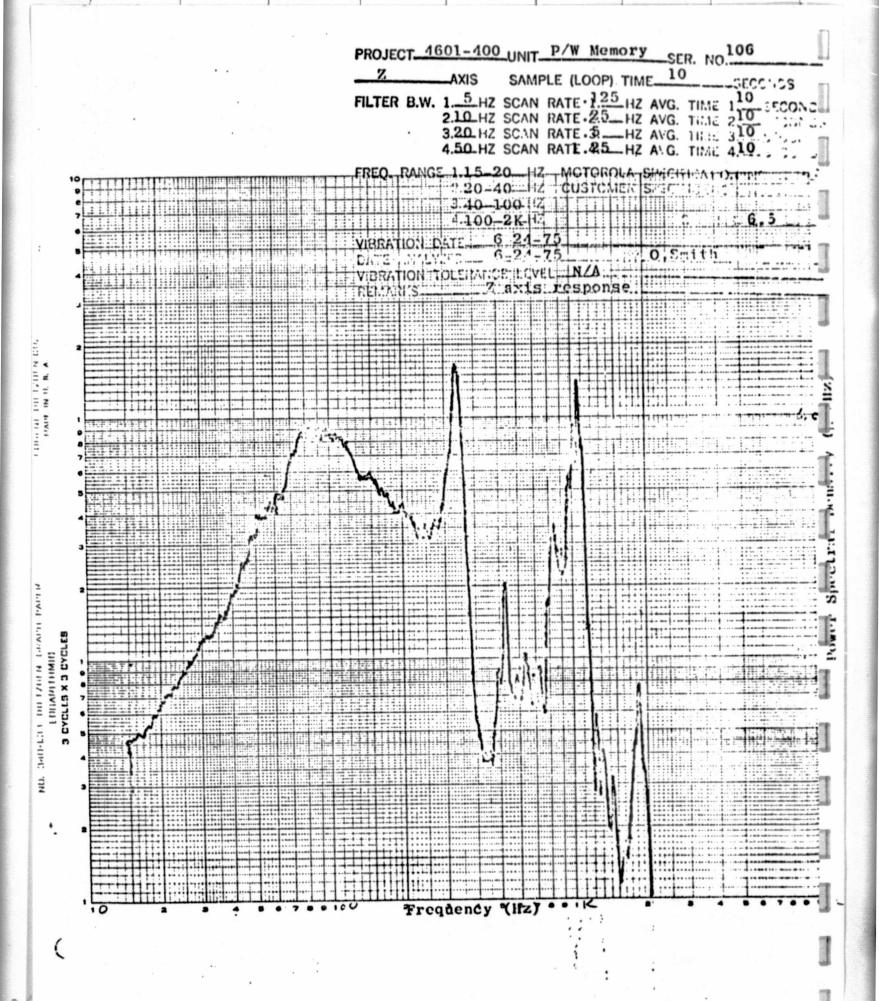


PH

X..._ __AXIS SAMPLE (LOOP) TIME_10_ FILTER B.W. 1.5 HZ SCAN RATE 1.125 IZ A.G. TIME 1.10SECONDS 2.10 HZ SCAN RATE 3.25 HZ A.G. TIME 2.10SECONDS 3.20 HZ SCAN RATE 3.5 HZ A.G. TIME 3.10SECONDS 4.50 HZ SCAN RATE14.25 HZ A G. TIME 4. 103ECONDS 15-20 HZ MOTORC A STORE NO. FREQ. RANGE 40-100 H4---1.100+2K-1:2---VIBRATION DATE 6-24-75 PEWARKS | X axis response Densi Frequency (Hz) APTONAL PAGE S POOR QUALITY

PROJECT-4601-400 UNIT P/W Memory SER. NO. 106





Date - 18.75 Model WIRE W.O. 3039 CONTROL 41 Serial HIGH VACUUM TEST Observer EE GOULDEN Vacuum System No. PRESSURE REMARKS TIME (mm Hg A) START TO HI VAC VEUT TO Arm. 5:20 1x 10-5 END TEST MOTOROLA/GED KO156 1/60 Page / of

PROJECT 4601-400 TYPE OF TEST  DATE 18 fine 75 SI MODULAR IMPACT  SHEET 1 OF 1 DEREE FALL DROP  W.O. NO. 3040  CONTROL NO. 1'  UNIT CRAtical When Memory  SERIAL NO. 10C  OPERATOR Ate Monitory  VIBRATION MOUNTS NONE  NO. OF DROPS PER PRESE 40 Library  TOTAL NO. OF DROPS  ACCELERATION 30 G'S  PULSE DURATION 6+12 MS  SPEC DETAILS 12-713722D as revived by Motocla-Stam from her Souther  BANDPASS FILTER 22 LOW FR. Hz  HAD AND PLATE CONFIGURATION  TYPE OF WAVESHAPE 12 STATE STATE  HAD AND PLATE CONFIGURATION  THE OF WAVESHAPE 12 STATE STATE  HAD AND PLATE CONFIGURATION  THE OF WAVESHAPE 12 STATE STATE  HAD AND PLATE CONFIGURATION  THE OF WAVESHAPE 12 STATE STATE  HAD AND PLATE CONFIGURATION  THE OF WAVESHAPE 12 STATE STATE  HAD AND PLATE CONFIGURATION  THE OF WAVESHAPE 12 STATE  HAD AND PLATE CONFIGURATION  THE OF WAVESHAPE 12 STATE  HAD AND PLATE CONFIGURATION  THE OF WAVESHAPE 12 STATE  THE OF STATE  THE	PROJECT 4601-400 TYPE OF TEST  DATE 18 fune 75 DMODULAR IMPACT  SHEET 1 OF 1 DFREE FALL DROP  W.O. NO. 3040  CONTROL NO. 10C  OPERATOR Ste Month  OBSERVER No. 10C  VIBRATION MOUNTS NONE  NO. OF DROPS PER FACE 484 Sour TOTAL NO. OF DROPS  ACCELERATION 30 G'S	1
DATE 18 fame 75 SMODULAR IMPACT SHEET 1 OF 1 DFREE FALL DROP  W.O. NO. 3040  CONTROL NO. 1'  UNIT CLASSIFIED WAS ENABLED TO TOTAL NO. OF DROPS  SERIAL NO. 10C  OBSERVER A Kee Shouldin  VIBRATION MOUNTS NONE  NO. OF DROPS PER FACE See Industry TO TOTAL NO. OF DROPS  ACCELERATION 30 G'S  PULSE DURATION 6 +1 2 MS  SPEC DETAILS 12-2137220 as revived by Motorba- Sham from her Shouldin  DROP HEIGHT 1 + 31 IN.  PROGRAMMER PRESSURE N17 PS.1.  TYPE OF WAVESHAPE NIM SAME  BANDPASS FILTER 2 LOW FR. Hz  #300 HIGH FR. Hz  #300 HIGH FR. Hz  #300 HIGH FR. Hz  #300 HIGH FR. Hz  #31 I MAR 2755 I will open B  ALL 2357 alum parts B	DATE 18 fine 75 DMODULAR IMPACT SHEET 1 OF 1 DFREE FALL DROP  W.O. NO. 3040  CONTROL NO. 1'  UNIT Okation When Memory  SERIAL NO. 10C  OPERATOR Ste Martin  OBSERVER Stee Souldin  VIBRATION MOUNTS NONE  NO. OF DROPS PER FACE 40x 1-low TOTAL NO. OF DROPS  ACCELERATION 30 G'S	Bogol Bogol
DATE 18 fame 75 SMODULAR IMPACT SHEET 1 OF 1 DFREE FALL DROP  W.O. NO. 3040  CONTROL NO. 1'  UNIT CLASSIFIED WAS ENABLED TO TOTAL NO. OF DROPS  SERIAL NO. 10C  OBSERVER A Kee Shouldin  VIBRATION MOUNTS NONE  NO. OF DROPS PER FACE See Industry TO TOTAL NO. OF DROPS  ACCELERATION 30 G'S  PULSE DURATION 6 +1 2 MS  SPEC DETAILS 12-2137220 as revived by Motorba- Sham from her Shouldin  DROP HEIGHT 1 + 31 IN.  PROGRAMMER PRESSURE N17 PS.1.  TYPE OF WAVESHAPE NIM SAME  BANDPASS FILTER 2 LOW FR. Hz  #300 HIGH FR. Hz  #300 HIGH FR. Hz  #300 HIGH FR. Hz  #300 HIGH FR. Hz  #31 I MAR 2755 I will open B  ALL 2357 alum parts B	DATE 18 fine 75 DMODULAR IMPACT SHEET 1 OF 1 DFREE FALL DROP  W.O. NO. 3040  CONTROL NO. 1'  UNIT Okation When Memory  SERIAL NO. 10C  OPERATOR Ste Martin  OBSERVER Stee Souldin  VIBRATION MOUNTS NONE  NO. OF DROPS PER FACE 40x 1-low TOTAL NO. OF DROPS  ACCELERATION 30 G'S	10.4
SHEET / OF / OF / OF PREE FALL DROP  W.O. NO. 3040  CONTROL NO. 1'  UNIT CLASTIC When Memory  SERIAL NO. 10C  OPERATOR CITE Mostin  OBSERVER & Kee Gouldin  VIBRATION MOUNTS NONE  NO. OF DROPS PER RICE 40 Low TOTAL NO. OF DROPS  ACCELERATION 30 G'S  PULSE DURATION 6+12 MS  SPEC DETAILS 2-7137220 as reviewly Motorola- Ham from her Souldin  Nisted 6-18-75  DROP HEIGHT -1 + 31 IN.  PROGRAMMER PRESSURE N/1 P.S.I.  TYPE OF WAVESHAPE IN A SUMMER PRESSURE N/1 P.S.I.  TYPE OF WAVESHAPE IN A SUMMER PRESSURE N/1 P.S.I.  AND HIGH FR. Hz  4300 HIGH FR. Hz  6 MS 2 MRL 2357 alum plant B  13 Superat 6 MS and 3drops at 12 MS  24 MRL 2357 alum plant B  13 Superat 6 MS and 3drops at 12 MS  25 MRL 2357 alum plant B  10 MRL 2357 alum plant B  11 MILLE AND RESERVEN  12 MRL 2357 alum plant B  13 Superat 6 MS and 3drops at 12 MS  14 MRL 2357 alum plant B  15 MRL 2357 alum plant B  16 MS 12 MS 12 MS  17 MRL 2357 alum plant B  18 MS 1 MRL 2357 alum plant B  19 MRL 2357 alum plant B  19 MRL 2357 alum plant B  10 MRL 2357 alum plant B  10 MRL 2357 alum plant B  11 MRL 2357 alum plant B  11 MRL 2357 alum plant B  12 MRL 2357 alum plant B  13 MRL 2357 alum plant B  14 MRL 2357 alum plant B  18 MS 1 MRL 2357 alum plant B  19 MRL 2357 alum plant B  19 MRL 2357 alum plant B  10 MRL 2357 alum plant B  10 MRL 2357 alum plant B  10 MRL 2357 alum plant B  11 MRL 2357 alum plant B  12 MRL 2357 alum plant B  13 MRL 2357 alum plant B  14 MRL 2357 alum plant B  15 MRL 2357 alum plant B  16 MRL 2357 alum plant B  17 MRL 2357 alum plant B  18	SHEET OF OF OF OF FREE FALL DROP  W.O. NO. 3040  CONTROL NO. 1'  UNIT Otatic War Meaning  SERIAL NO. 106  OPERATOR Othe Houldin  VIBRATION MOUNTS NONE  NO. OF DROPS PER FACE 40 Low TOTAL NO. OF DROPS  ACCELERATION 30 G'S	500
WO. NO. 3040  CONTROL NO. 1'  UNIT CLATED Were Memory  SERIAL NO. 10C  OPERATOR Stree Month  OBSERVER Stree Stown TOTAL NO. OF DROPS  VIBRATION MOUNTS  NO. OF DROPS PER FACE LEVE LOW TOTAL NO. OF DROPS  CACCELERATION 30 G'S  PULSE DURATION 6+12 MS  SPEC DETAILS 15-213722D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-213722D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-213722D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-213722D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-213722D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-213722D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-213722D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-213722D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-213722D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-213722D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-213722D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-213722D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-213722D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-213722D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-213722D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-213722D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-213722D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-213722D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-213722D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-213722D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-213722D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-21372D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-21372D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-21372D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-21372D as revived by Motrola- Stam from her Souldhan  SPEC DETAILS 15-21372D as	CONTROL NO. 1' UNIT	1
CONTROL NO. 10 C  UNIT CLATED When Memory  SERIAL NO. 10 C  OPERATOR Ste Martin  OBSERVER Stee Shouldin  VIBRATION MOUNTS NONE  NO. OF DROPS PER FACE 400 Sour TOTAL NO. OF DROPS  ACCELERATION 30 G'S  PULSE DURATION 6+12 MS  SPEC DETAILS 12-213722D as revicely Motivola- Stam from he Souldin  DROP HEIGHT 1/2 + 3/2 IN.  PROGRAMMER PRESSURE N/2 P.S.I.  TYPE OF WAVESHAPE Not Source Source Source Stam from he Souldin  TYPE OF WAVESHAPE Not Source Sourc	UNIT	22.1
UNIT Clatic Were Menory  SERIAL NO. 106  OPERATOR Ste Mouldin  VIBRATION MOUNTS NONE  NO. OF DROPS PER LITTLE LOW LOW TOTAL NO. OF DROPS  ACCELERATION 30 G'S  PULSE DURATION 6+12 MS  SPEC DETAILS 15-2/37220 as reviewly Motrola- Gram from her Gouldin  KIRCLE 6-18-75  DROP HEIGHT 1/2 + 3/2 IN.  PROGRAMMER PRESSURE N/2 P.S.I.  TYPE OF WAVESHAPE MIN SILVE  BANDPASS FILTER 2 LOW FR. Hz  4300 HIGH FR. Hz  FREMARKS  1) 31 MAR 2357 alum patt B  1) 31 MAR 2357 alum patt B  1) 11 8888 2 Route  ALERTA ON DESCRIPTION  1 81888 2 Route  6 2 888 XY Marthia  1 1 1 Reclared  6 1 1" Muse aplan  1 1" Muse aplan	UNIT_CLATED Were Meanwry  SERIAL NO. 10C  OPERATOR Catte Martin  OBSERVER & Kee Souldin  VIBRATION MOUNTS NONE  NO. OF DROPS PER FACE SEE Islaw TOTAL NO. OF DROPS  ACCELERATION 30 G'S	J
SERIAL NO. 10C  OPERATOR Ste Mother  OBSERVER & Kee Gouldin  VIBRATION MOUNTS NONE  NO. OF DROPS PER STEE 402 (Now TOTAL NO. OF DROPS  ACCELERATION 30 G'S  PULSE DURATION 6+12 MS  SPEC DETAILS 12-2/37220 as reviewly Motrola- Gram from her Gouldin  Kittle 6-18-75  DROP HEIGHT -1. + 3/2 IN.  PROGRAMMER PRESSURE NI P.S.I.  TYPE OF WAVESHAPE AND SILL AND PLATE CONFIGURATION  TYPE OF WAVESHAPE AND SILL AND PLATE CONFIGURATION  TYPE OF WAVESHAPE AND SILL	OPERATOR Citte Matter  OBSERVER A Kee Souldin  VIBRATION MOUNTS NONE  NO. OF DROPS PER FACE 46x Islam TOTAL NO. OF DROPS  ACCELERATION 30 G'S	5,
OPERATOR Stee Matter  OBSERVER A Lee Souldin  VIBRATION MOUNTS NONE  NO. OF DROPS PER FACE 40x I low TOTAL NO. OF DROPS  C  ACCELERATION 30 G'S  PULSE DURATION 6+12 MS  SPEC DETAILS 12-713722D as reviewly Motorola- Gram from Lee Souldin  Extend 6-18-75  DROP HEIGHT 1-1 TOTAL NO. OF DROPS  DROP HEIGHT 1-1 TOTAL NO. OF DROPS  C  DROP HEIGHT 1-1 TOTAL NO. OF DROPS  OF PAD AND PLATE CONFIGURATION  TYPE OF WAVESHAPE Not P.S.I.  TYPE OF WAVESHAPE 10 Source So	OPERATOR Citte Motter  OBSERVER No. OF DROPS PER FACE see Islam TOTAL NO. OF DROPS  ACCELERATION 30 G'S	
OBSERVER of the Soulding VIBRATION MOUNTS NONE  NO. OF DROPS PER FACE LEW FOUR TOTAL NO. OF DROPS  ACCELERATION 30 G'S  PULSE DURATION 6+12 MS  SPEC DETAILS 12-213722D as revived by Motorola- Sham from her Soulding Stated 6-18-75  DROP HEIGHT -1 + 31/2 IN.  PROGRAMMER PRESSURE NIT P.S.I.  TYPE OF WAVESHAPE Source 1 LOW FR. Hz  #300 HIGH FR. Hz  FAMARKS  1) 31 mg of 6 MS and 3drops at 12 ms  SINGULATION DESCRIPTION  1 MRL 2357 alum plate  1 MRL 2357 alum parts  B  2 MRL 2357 alum parts  B  3 MRL 2357 alum parts  B  3 MRL 2357 alum parts  B  4 MRL 2357 alum pa	VIBRATION MOUNTS NONE  NO. OF DROPS PER FACE SEX ISLOW TOTAL NO. OF DROPS  ACCELERATION 30 G'S	1004
VIBRATION MOUNTS NONE  NO. OF DROPS PER FACE 40 / Low TOTAL NO. OF DROPS C  ACCELERATION 30 G'S  PULSE DURATION 6+12 MS  SPEC DETAILS 12-713722D as reviewly Motorola- Gram from Lee Goulden Kintel 6-18-75  DROP HEIGHT 1/2 + 3/2 IN.  PROGRAMMER PRESSURE N/1 P.S.I.  TYPE OF WAVESHAPE 10 LOW FR. Hz  4300 HIGH FR. Hz  REMARKS  13 1 MRL 23579 alum parts B  14 1 MRL 23579 alum parts B  15 1 8x8x2 from the C. axis  16 2 8x8x2 from the C. axis  17 3 8x3x2 from the C. axis  18 3 1 1 Street Lowed  19 1 1 Street Lowed  10 1 1 Street Lowed  10 1 1 Street Lowed  11 1 Street Lowed  12 1 MS  13 1 MS  14 1 Street Lowed  15 1 8x8x2 from the C. axis  16 2 8x8x2 from the C. axis  17 3 8x3x2 from the C. axis  18 3 1 Street Lowed  19 1 1 Street Lowed  10 1 1 Street Lowed	NO. OF DROPS PER FACE SEE LACE TOTAL NO. OF DROPS C  ACCELERATION 30 G'S	100
NO. OF DROPS PER FACE 4ex four TOTAL NO. OF DROPS  ACCELERATION 30 G'S  PULSE DURATION 6+12 MS  SPEC DETAILS 12-7137220 as reviewly Motorola- Lam from her Loudden  DROP HEIGHT -1/- + 31/2 IN.  PROGRAMMER PRESSURE N/7 P.S.I.  TYPE OF WAVESHAPE June Simul ITEM PART NO. DESCRIPTION  BANDPASS FILTER 27 LOW FR. Hz  4300 HIGH FR. Hz  REMARKS  13 1 MRL 2359 alum parts B  13 1 MRL 2359 alum parts B  14 13 8x8x 1/2 restore  GES 12 MS 8x8 1/2 restore  13 8x8x 1/2 restore  14 3 8x8x 1/2 restore  15 1 8x8x 1/2 restore  16 2 8x8x 1/2 restore  17 3 8x8x 1/2 restore  18 3 1" therefored  19 1 1" blue aplan	NO. OF DROPS PER FACE SEE Labour TOTAL NO. OF DROPS	-
ACCELERATION 30 G'S  PULSE DURATION 6+12 MS  SPEC DETAILS 12-213722.D as reviewly Motorola- Sham from Lee Soulden  BANDPHEIGHT 1/1 + 3/2 IN.  PROGRAMMER PRESSURE N/7 P.S.I.  IYPE OF WAVESHAPE 10 LOW FR. Hz  4300 HIGH FR. Hz  FREMARKS  1) 31 year of 6 HS and 3 drops at 12 HS  When the an deletime test calle.  6 2 888 NS rubbins  6 2 888 NS rubbins  6 3 888 NS rubbins  6 3 1" Hueclosed  8 3 1" Hueclosed  9 1 1" Hue appen	ACCELERATION 30 G'S	
PULSE DURATION 6+12 MS  SPEC DETAILS 15-2137220 as revively Motorola- Sham from Lee Soulden  DROP HEIGHT 1/2 + 3/2 IN.  PROGRAMMER PRESSURE N/1 P.S.I.  TYPE OF WAVESHAPE and serve  BANDPASS FILTER 22 LOW FR. Hz  4300 HIGH FR. Hz  GMS 12 MRL 2795 1 red open B  REMARKS  (1) 31 years 6 MS and 3drops at 12 ms  Alee to an defetime test cable.  But to an defetime test cable.  GMS 13 MS  GMS 12 MS  10 MS 12 MS  11 Superior 2 Company of the Cyarus  12 MS 12 MS 12 MS  13 MS 12 MS  14 MS 12 MS  15 Hereclosed  16 HS 17 Hereclosed  16 HS 17 Hereclosed  16 HS 17 Hereclosed  17 Hereclosed	( 2	
SPEC DETAILS 12-213722D as reviewly Motorola- Stam from her Smilling Minted 6-18-75  DROP HEIGHT 1/2 + 3/2 IN.  PROGRAMMER PRESSURE N/7 P.S.I.  TYPE OF WAVESHAPE 10 A STAND DESCRIPTION  BANDPASS FILTER 22 LOW FR. Hz  4300 HIGH FR. Hz  GHS 2 MRL 2755 1" red open B  REMARKS  1) 31 year 16 MS and 3drops at 12 ms  1) 11 MS PART NO. DESCRIPTION  1 MRL 2755 1" red open B  13 MRL 2357 alum parts B  1) 31 year 16 MS and 3drops at 12 ms  1) 11 MS PART NO. DESCRIPTION  1 MRL 2755 1" red open B  1 MRL 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX MS PART 2357 alum parts B  1 MS SX SX	SPEC DETAILS 12-2137220 as revised by Motorola- Sham from Lee Soulden	100
DROP HEIGHT 1/2 + 3/2 IN.  PROGRAMMER PRESSURE N/7 P.S.I.  IYPE OF WAVESHAPE 1 LOW FR. HZ  BANDPASS FILTER 2 LOW FR. HZ  4300 HIGH FR. HZ  REMARKS  (1) 3! 1 1 1 6 HS and 3 drops at 12 HS  (2) 11 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		_
PROGRAMMER PRESSURE  N/t - P.S.I.  IYPE OF WAVESHAPE  BANDPASS FILTER  2 LOW FR. Hz  4300 HIGH FR. Hz  REMARKS  (1) 31 year of 6 HS and 3drops at 12 HS  (2) MRL 2359 alum parts  (3) MRL 2359 alum parts  B  (4) It, reserve 2-6 ms drops on the C, ares  Gue to an defection test cable.  (6) 48 88 8 X X restrict  (6) 13 8 8 8 X X restrict  (6) 14 8 8 8 X X restrict  (7) 3 8 8 8 X X restrict  (8) 3 1" I blue copen  (9) 1 1" blue copen	diaxed 6-18-75	-
PROGRAMMER PRESSURE  IVIT P.S.I.  ITHE OF WAVESHAPE  BANDPASS FILTER  2 LOW FR. Hz  4300 HIGH FR. Hz  REMARKS  I) 31 year 16 HS and 3drops at 12 ms  A Street 2-6ms drops on the Crakes  Augustian detection that calle.  Band 12 HS  Band And Plate configuration  DESCRIPTION  MRL 2577 alum plate T  A REMARKS  I) 11 year 16 HS and 3drops at 12 ms  A Street and better that calle.  Band Band And Band An	DROP HEIGHT 3/4 + 3/2 IN.	
TYPE OF WAVESHAPE  BANDPASS FILTER  2- LOW FR. Hz  4300 HIGH FR. Hz  REMARKS  (1) 3! year of 6 HS and 3 drops at 12 HS  (2) MRL 2359 alum parte B  (3) MRL 2359 alum parte B  (4) MRL 2514 alum parte B  (5) MRL 2359 alum parte B  (6) MRL 2359 alum parte B  (7) MRL 2359 alum parte B  (8) MRL 2359 alum parte B  (9) MRL 2359 alum parte B  (1) 3! year of 6 HS and 3 drops at 12 HS  (1) MRL 2359 alum parte B  (2) MRL 2359 alum parte B  (3) MRL 2359 alum parte B  (4) MRL 2745 I red open B  (5) MRL 2359 alum parte B  (6) MRL 2745 I red open B  (6) MRL 2745 I red open B  (6) MRL 2745 I red open B  (7) MRL 2745 I red open B  (8) MRL 2359 alum parte B  (8) MRL 2359 alum parte B  (8) MRL 2359 alum parte B  (9) MRL 2745 I red open B  (1) MRL 2745 I red open B  (1) MRL 2745 I red open B  (2) MRL 2359 alum parte B  (3) MRL 2359 alum parte B  (4) MRL 2745 I red open B  (5) MRL 2359 alum parte B  (6) MRL 2745 I red open B  (6) MRL 2745 I red open B  (7) MRL 2745 I red open B  (8) MRL 2359 alum parte B  (8) MRL 2359 alum parte B  (8) MRL 2359 alum parte B  (9) MRL 2745 I red open B  (1) MRL 2745 I red open B  (1) MRL 2745 I red open B  (2) MRL 2359 alum parte B  (3) MRL 2359 alum parte B  (4) MRL 2745 I red open B  (5) MRL 2745 I red open B  (6) MRL 2745 I red open B  (7) MRL 2745 I red open B  (8) MRL 2755 I red open B  (9) MRL 2755 I red open B  (9) MRL 2755 I red open B  (1) MRL 2755 I red open B  (1) MRL 2755 I red open B  (1) MRL 2755 I red open B  (2) MRL 2755 I red open B  (3) MRL 2359 alum parte B  (4) MRL 2755 I red open B  (5) MRL 2755 I red open B  (6) MRL 2755 I red open B  (7) MRL 2755 I red open B  (8) MRL 2755 I red open B  (8) MRL 2755 I red open B  (9) MRL 2755 I red open B  (9) MRL 2755 I red open B  (1) MRL 2755 I red open B  (1) MRL 2755 I red open B  (1) MRL 2755 I red open B  (2) MRL 2755 I red open B  (3) MRL 2755 I red open B  (4) MRL 2755 I red open B  (5) MRL 2755 I red open B  (6) MRL 2755 I red open B  (7) MRL 2755 I red op		1
BANDPASS FILTER 2 LOW FR. Hz  4300 HIGH FR. Hz  REMARKS  (3 MRL 2785 1" red open B  (3 MRL 2359 alum parte B  (4) 31 years 16 MS and 3drops at 12 MS  (4) MRL 2359 alum parte B  (5) MRL 2359 alum parte B  (6) MRL 2359 alum parte B  (7) MRL 2785 1" red open B  (8) MRL 2359 alum parte B  (8) MRL 2359 alum parte B  (9) MRL 2785 1" red open B  (1) 31 years 16 MS and 3drops at 12 MS  (1) 31 years 16 MS and 3drops at 12 MS  (2) MRL 2785 1" red open B  (3) MRL 2785 1" red open B  (4) MRL 2785 1" red open B  (4) MRL 2785 1" red open B  (5) MRL 2785 1" red open B  (6) MRL 2785 1" red open B  (7) MRL 2785 1" red open B  (8) MRL 2785 1" red open B  (9) MRL 2785 1" red open B  (	1774	
REMARKS  (3) MRC 2359 alum parte B  (1) 3! year 16 45 and 3drops at 12 ms  (3) MRC 2359 alum parte B  (4) MRC 2359 alum parte B  (5) MRC 2359 alum parte B  (6) MRC 2359 alum parte B  (7) MRC 2359 alum parte B  (8) MRC 2359 alum parte B	BANDPASS FILTER . 2. LOW FR. Hz [ MRL 25) 4 alum plate T	1000
REMARKS  (1) 31 year of 6 MS and 3 drops at 12 MS  (2) MRI 2359 alum parte B  (3) MRI 2359 alum parte B  (4) Stream and 3 drops at 12 MS  (5) It 8x8x / charter  (6) Exercise 2-6 MS drops and the Cracks  (6) Les xx / xx	4300 HIGH FR. Hz 645 72 MRL 2785 1"red open B	
1) 3! ye at 6 HS and 3drops at 12 HS  1) The server 2-6 MS drops on the C, axes  6 2 8x8 x y rubber  7 3-8x3 x 16 rubber  8 3-1" Hue closed  9 1-1" blue apen	REMARKS (3 MRC 2359 alum parte B	-
die to an defection text cable.  6 2 8x8x 1/8 rubbin  7 3 8x8x 1/8 rubbin  8 3 1" the closed  9 1 1" blue upon	1) 31 me at 6 45 and 3 drops at 12 ms 4	-
7 3- 8×5× 16 rubture  8 3- 1" the closed  9 1- 1" thue apen	=) therewere 2-6ms drops on the Cakes 5 1- 8x8x3 plante	
7 3- 8×5× 16 rubture  8 3- 1" the closed  9 1- 1" thue apen	die to an defection test cable. 6 2- 8x8x 18 rubbies	65
8 3- 1" Hue closed 9 1- 1" Hue closed	7 3- 8×3× 26 rections	
G43 1343		
G43 1343	1 1 1" blue apen	
AXIS FACE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20	GHS 12 MS	
	AXIS FACE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19	ю
, x   X   X	, x   x   x	_
		490

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2